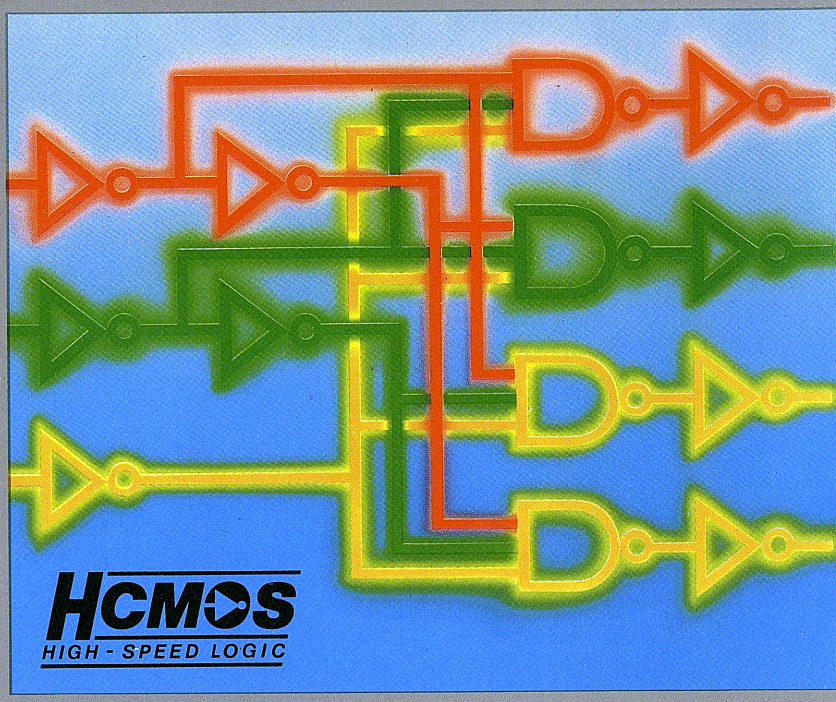
Designer's Guide

High-speed CMOS

January 1986



PHILIPS
Electronic
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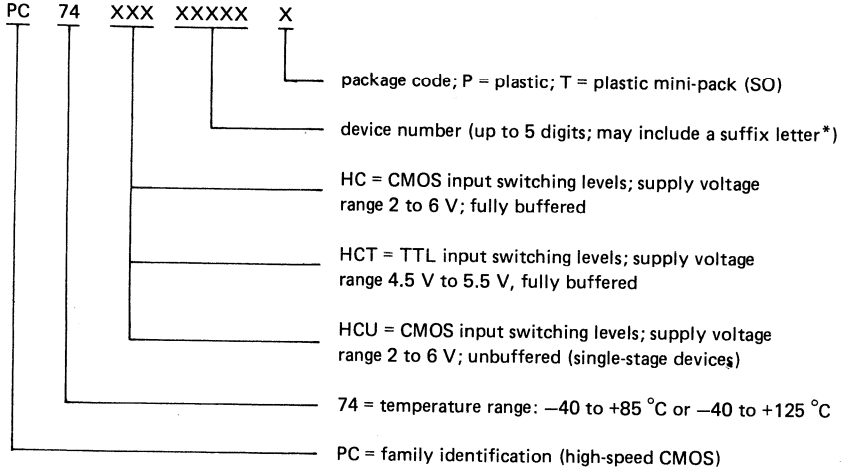
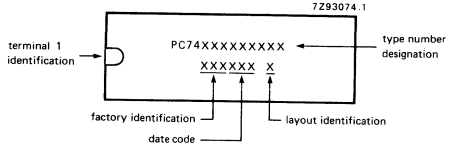
ORDERING INFORMATION

TYPE NUMBER DESIGNATIONS





* Example suffix "B": this type has bus driver output capability in contrast with the plane version.

DESIGNER'S GUIDE

INTRODUCTION

INTRODUCTION FOR THE HCMOS DESIGNER'S GUIDE

This guide has been prepared to provide an understanding of the principles involved in the design of systems using our 74HC/HCT/HCU family of high-speed CMOS (HCMOS) logic ICs. Design examples and performance are given for a wide variety of HCMOS applications, together with methods of protecting HCMOS when it is used in the automotive environment. General circuit board construction principles are also given, covering subjects such as power supply decoupling, interfacing and protection of circuit board inputs. The guide also covers important subjects such as handling, quality, and using HCMOS to replace LSTTL to reduce power consumption without loss of speed. The HCMOS family specification, comprehensive lists of available logic functions and an explanation of the new IEC logic symbols are also included.

The wealth of information contained within this guide is primarily intended for the use of logic circuit and system designers but will also be invaluable to technicians, students and others interested in obtaining a deeper understanding of HCMOS ICs so they can fully exploit their outstanding performance.

HCMOS FAMILY CHARACTERISTICS

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.
However, to be totally safe, it is desirable to take handling precautions into account (see also chapter "HANDLING PRECAUTIONS").

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 10 V is specified as the maximum operating voltage.

RECOMMENDED OPERATING CONDITIONS FOR 74HCU

SYMBOL	PARAMETER	74HCU			UNIT	CONDITIONS
		min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	V	
V_I	DC input voltage range	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	°C	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current — standard outputs — bus driver outputs		 25 35	 mA mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with: — standard outputs — bus driver outputs		 50 70	 mA mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT/HCU
	plastic DIL		500	mW	above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 11 V is specified as the maximum operating voltage.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage all outputs		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
V_{OL}	LOW level output voltage bus driver outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current **SSI** **flip-flops** **MSI**			 2.0 4.0 8.0		 20.0 40.0 80.0		 40.0 80.0 160.0	 μA μA μA	 6.0 6.0 6.0	 V_{CC} or GND	 $I_O = 0$ $I_O = 0$ $I_O = 0$

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage all outputs	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage all outputs		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
V_{OL}	LOW level output voltage bus driver outputs		0.16	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current **SSI** **flip-flops** **MSI**			 2.0 4.0 8.0		 20.0 40.0 80.0		 40.0 80.0 160.0	 μA μA μA	 5.5 5.5 5.5	V_{CC} or GND	 $I_O = 0$ $I_O = 0$ $I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V_I = 2.4 V; V_{CC} = 5.5 V) specification is: ΔI_{CC} = 0.65 mA (typical) and 1.8 mA (maximum) across temperature.

DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCU								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.7 3.6 4.8	1.4 2.6 3.4		1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.6 1.9 2.6	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.8 4.0 5.5	2.0 4.5 6.0		1.8 4.0 5.5		1.8 4.0 5.5		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{CC} or GND	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage		0 0 0	0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{CC} or GND	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current SSI			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	$I_O = 0$

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time standard outputs		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 3 and 4
t_{THL}/ t_{TLH}	output transition time bus driver outputs		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 3 and 4

AC CHARACTERISTICS FOR 74HCU

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCU								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 1

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{THL}/ t_{TLH}	output transition time standard outputs		7	15		19		22	ns	4.5	Figs 8 and 9
t_{THL}/ t_{TLH}	output transition time bus driver outputs		5	12		15		18	ns	4.5	Figs 8 and 9

HCU TYPES

AC WAVEFORMS 74HCU

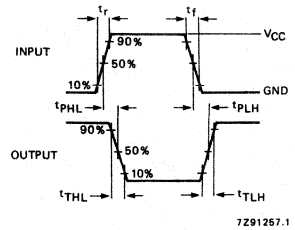


Fig. 1 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

TEST CIRCUIT FOR 74HCU

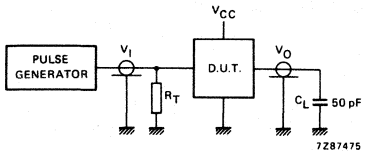


Fig. 2 Test circuit.

Definitions for Fig. 2:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HC TYPES

AC WAVEFORMS 74HC

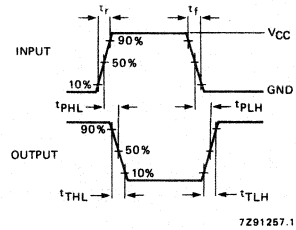


Fig. 3 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC WAVEFORMS 74HC

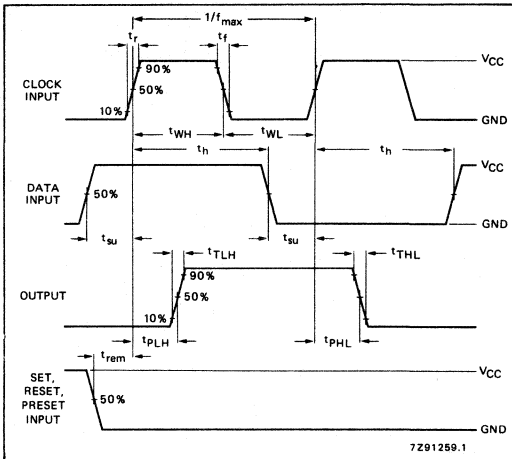


Fig. 4 Set-up times, hold times, removal times, propagation delays and the maximum clock pulse frequency for sequential logic ICs.

Notes to Fig. 4

1. In Fig. 4 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.
2. For AC measurements: $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

HC TYPES (continued)

TEST CIRCUIT FOR 74HC

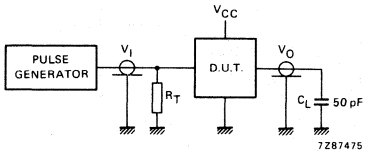


Fig. 5 Test circuit.

Definitions for Fig. 5:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

AC WAVEFORMS 74HC (continued)

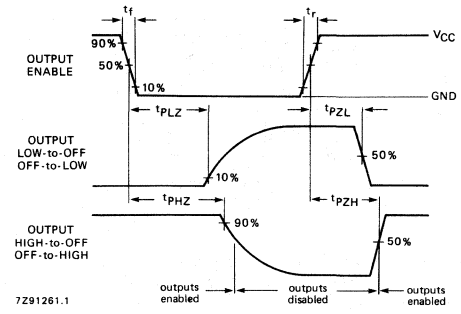
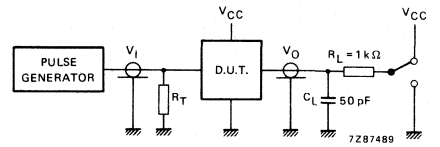


Fig. 6 Propagation delays of 3-state outputs.

TEST CIRCUIT FOR 74HC



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Note to switch position table

For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

Fig. 7 Test circuit for 3-state outputs.

Definitions for Fig. 7:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HCT TYPES

AC WAVEFORMS 74HCT

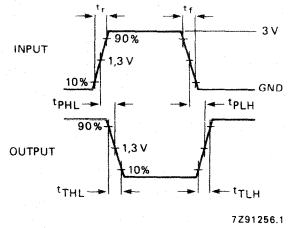


Fig. 8 Input rise and fall times, transition times and propagation delays for combinatorial logic ICs.

AC WAVEFORMS 74HCT

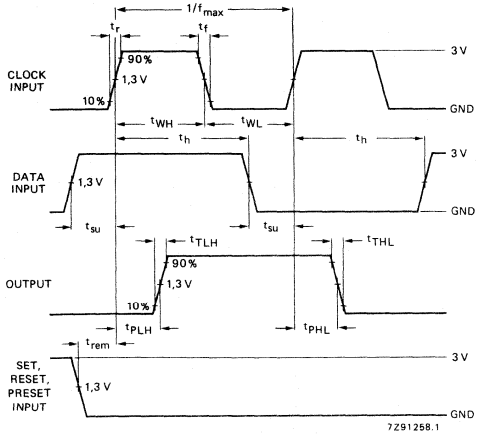


Fig. 9 Set-up times, hold times, removal times, propagation delays and the maximum clock pulse frequency for sequential logic ICs.

Notes to Fig. 9

1. In Fig. 9 the active transition of the clock is going from LOW-to-HIGH and the active level of the forcing signals (SET, RESET and PRESET) is HIGH. The actual direction of the transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.
2. For AC measurements: $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

TEST CIRCUIT FOR 74HCT

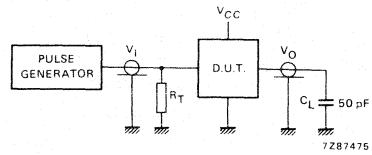


Fig. 10 Test circuit.

Definitions for Fig. 10:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

HCT TYPES (continued)

AC WAVEFORMS 74HCT (continued)

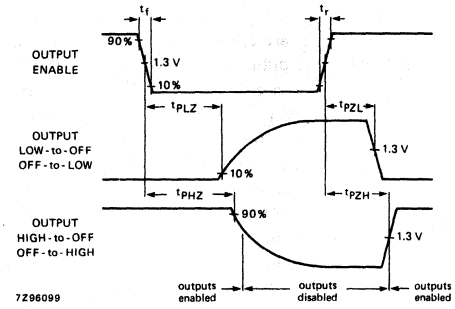
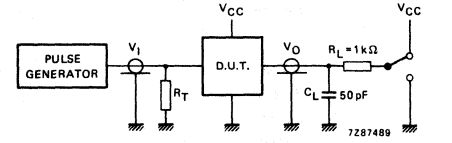


Fig. 11 Propagation delays of 3-state outputs.

TEST CIRCUIT FOR 74HCT



Switch position

TEST	SWITCH
t_{PZH}	GND
t_{PZL}	V_{CC}
t_{PHZ}	GND
t_{PLZ}	V_{CC}

Note to switch position table

For open-drain N-channel outputs t_{PLZ} and t_{PZL} are applicable.

Fig. 12 Test circuit for 3-state outputs.

Definitions for Fig. 12:

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).
R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

INTRODUCTION

The 74HCMOS data sheets have been designed for ease-of-use. A minimum of cross-referencing for more information is needed.

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of t_{PLH} and t_{PHL} for the longest data path through the device with a 15 pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on t_r and t_f.

LOGIC SYMBOLS

Two logic symbols are given for each device — the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEC Logic Symbol as developed by the IEC (International Electrotechnical Commission).

The IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) which supersedes Publication 117-15, published in 1972.

RATINGS

The "RATINGS" table (Limiting values in accordance with the Absolute Maximum System — IEC134) lists the maximum limits to which the device can be subjected without damage. This doesn't imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life won't have been shortened.

The maximum rated supply voltage of 7 V is well below the typical breakdown voltage of 18 V.

RECOMMENDED OPERATING CONDITIONS

The "RECOMMENDED OPERATING CONDITIONS" table lists the operating ambient temperature and the conditions under which the limits in the "DC CHARACTERISTICS" and "AC CHARACTERISTICS" tables will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC CHARACTERISTICS tables.

DC CHARACTERISTICS

The "DC CHARACTERISTICS" table reflects the DC limits used during testing. The values published are guaranteed.

The threshold values of V_{IH} and V_{IL} can be tested by the user. If V_{IH} and V_{IL} are applied to the inputs, the output voltages will be those published in the "DC CHARACTERISTICS" table. There is a tendency, by some, to use the published V_{IH} and V_{IL} thresholds to test a device for functionality in a "function-table exercizer" mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 metre. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use V_{IH} and V_{IL} to test the functionality of any HCMOS device type; instead, use input voltages of V_{CC} (for the HIGH state) and 0 V (for the LOW state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical V_{IL} is higher than the maximum V_{IL}. However, this is because V_{ILmax} is the maximum V_{IL} (guaranteed) for all devices that will be recognized as a logic LOW. However, typically a **higher** V_{IL} will also be recognized as a logic LOW. Conversely, the typical V_{IH} is lower than its minimum guaranteed level.

For 74HCMOS, unlike TTL, no output HIGH short-circuit current is specified. The use of this current, for example, to calculate propagation delays with capacitive loads, is covered by the HCMOS graphs showing the output drive capability and those showing the dependence of propagation delay on load capacitance.

The quiescent supply current I_{CC} is the leakage current of all the reversed-biased diodes and the OFF-state MOS transistors. It is measured with the inputs at V_{CC} or GND and is typically a few nA.

AC CHARACTERISTICS

The "AC CHARACTERISTICS" table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveforms section.

TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a ground-plane) should be used for the same reasons. A V_{CC} decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 6 ns, a signal swing of 0 V to V_{CC} for 74HC and 0 V to 3 V for 74HCT; a 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing f_{max}. Two pulse generators are usually required for testing such parameters as set-up time, hold time and removal time. f_{max} is also tested with 6 ns input rise and fall times, with a 50% duty factor, but for typical f_{max} as high as 60 MHz, there are no constraints on rise and fall times.

DEFINITIONS OF SYMBOLS AND TERMS USED IN HCMOS DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device.
Negative current is defined as conventional current flow out of a device.

I_{CC} Quiescent power supply current; the current flowing into the V_{CC} supply terminal.

ΔI_{CC} Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.

I_{GND} Quiescent power supply current; the current flowing into the GND terminal.

I_I Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.

I_{IK} Input diode current; the current flowing into a device at a specified input voltage.

I_O Output source or sink current; the current flowing into a device at a specified output voltage.

I_{OK} Output diode current; the current flowing into a device at a specified output voltage.

I_{OZ} OFF-state output current; the leakage current flowing into the output of a 3-state device in the OFF-state, when the output is connected to V_{CC} or GND.

I_S Analog switch leakage current; the current flowing into an analog switch at a specified voltage across the switch and V_{CC}.

Voltages

All voltages are referenced to GND (ground), which is typically 0 V.

GND Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{CC} Supply voltage; the most positive potential on the device.

V_{EE} Supply voltage; one of two (GND and V_{EE}) negative power supplies.

V_H Hysteresis voltage; difference between the trigger levels, when applying a positive and a negative-going input signal.

V_{IH} HIGH level input voltage ; the range of input voltages that represents a logic HIGH level in the system.

V_{IL} LOW level input voltage; the range of input voltages that represents a logic LOW level in the system.

V_{OH} HIGH level output voltage ; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} LOW level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

V_{T+} Trigger threshold voltage; positive-going signal.

V_{T-} Trigger threshold voltage; negative-going signal.

Analog terms

R_{ON} ON-resistance; the effective ON-state resistance of an analog switch, at a specified voltage across the switch and output load.

ΔR_{ON} ΔON-resistance; the difference in ON-resistance between any two switches of an analog device at a specified voltage across the switch and output load.

Capacitances

C_I Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$ Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).

C_L Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

C_{PD} Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function, when no extra load is provided to the device.

C_S Switch capacitance; the capacitance of a terminal to a switch of an analog device.

AC switching parameters

f_i Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.

f_o Output frequency; each output.

f_{max} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10%V_{CC} to 90%V_{CC} in accordance with the device function table.

t_h Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_r, t_f Clock input rise and fall times; 10% and 90% values.

AC switching parameters (continued)

t_{PHL} Propagation delay; the time between the specified reference points, normally the 50% points for 74HC and 74HCU devices on the input and output waveforms and the 1.3 V points for the 74HCT devices, with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH} Propagation delay; the time between the specified reference points, normally the 50% points for 74HC and 74HCU devices on the input and output waveforms and the 1.3 V point for the 74HCT devices, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHZ} 3-state output disable time; the time between the specified reference points, normally the 50% points for the 74HC and 74HCU devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a HIGH level (V_{OH}) to a high impedance OFF-state (Z).

t_{PLZ} 3-state output disable time; the time between the specified reference points, normally the 50% points for the 74HC devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and a point representing 10% of the output swing on the output voltage waveform of a 3-state device, with the output changing from a LOW level (V_{OL}) to a high impedance OFF-state (Z).

t_{PZH} 3-state output enable time; the time between the specified reference points, normally the 50% points for the 74HC devices and 1.3 V points for the 74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a HIGH level (V_{OH}).

t_{PZL} 3-state output enable time; the time between the specified reference points, normally the 50% points for the 74HC devices and the 1.3 V points for the 74HCT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state (Z) to a LOW level (V_{OL}).

t_{rem} Removal time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for 74HC devices and the 1.3 V points for the 74HCT devices on both input voltage waveforms.

t_{su} Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the coltrol input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH-to-LOW.

t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW-to-HIGH.

t_W Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for 74HC and 74HCU devices and at the 1.3 V points for 74HCT devices.

USER GUIDE

Note: The information in this user guide is intended as a design-aid and does not constitute a guarantee.

INTRODUCTION

The 74HC/HCT/HCU family is a comprehensive range of high-speed CMOS (HCMOS) integrated circuits. Whilst retaining all the advantages of CMOS technology - wide operating voltage range, very low power consumption, high input noise immunity and wide operating temperature range - these circuits have the high-speed and drive capabilities of low-power Schottky TTL (LSTTL). An extensive product range (most TTL functions and some devices from the successful HE4000B series: analog multiplexers, long time-constant multivibrators, phase-locked loops) and the aforementioned performance open new avenues in system design.

For comparison, the key performance parameters of HCMOS are shown with those of other technologies in Table 1. The propagation delay of metal-gate CMOS ruled out CMOS for many applications until the arrival of our HE4000B series. Now, our 3 μm gate HCMOS technology has a speed comparable to LSTTL while retaining the important CMOS qualities, see Fig.1.

Table 2 compares the operating characteristics of the 74HC and 74HCT IC types with those of LSTTL in more detail. 74HC and 74HCT devices are ideal for use in new equipment designs and, as alternatives to TTL devices, in existing designs. The 74HCT circuits which are direct replacements for LSTTL circuits also enhance performance in many respects.

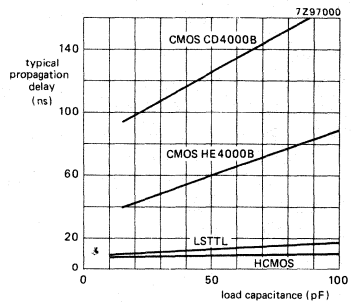


Fig. 1 Propagation delay as a function of load capacitance; V_{CC} = 5 V, T_{amb} = 25 °C.

Table 1 Comparison of CMOS and TTL technologies;
supply voltage V_{CC} = 5 V; ambient temperature T_{amb} = 25 °C; load capacitance C_L = 15 pF

parameters	technology	HCMOS	metal gate CMOS	standard TTL	low-power Schottky TTL	Schottky TTL	advanced low-power Schottky TTL	advanced Schottky TTL	Fairchild advanced Schottky TTL
	family	74HC	4000 CD HE	74	74LS	74S	74ALS	74AS	74F
Power dissipation, typ. (mW)									
Gate	static	0.0000025	0.001	10	2	19	1.2	8.5	5.5
	dynamic @ 100 kHz	0.075	0.1	10	2	19	1.2	8.5	5.5
Counter	static	0.000005	0.001	300	100	500	60	–	190
	dynamic @ 100 kHz	0.125	0.120	300	100	500	60	–	190
Propagation delay (ns)									
Gate	typical	8	94 40	10	9.5	3	4	1.5	3
	maximum	14	190 80	20	15	5	7	2.5	4
Delay/power product (pJ)									
Gate	at 100 kHz	0.52	9 4	100	19	57	4.8	13	16.5
Maximum clock frequency (MHz)									
D-type flip-flop	typical	55	4 12	25	33	100	60	160	125
	minimum	30	2 6	15	25	75	40	–	100
Counter	typical	45	2 6	32	32	70	45	–	125
	minimum	25	1 3	25	25	40	–	–	100
Output drive (mA)									
	standard outputs	4	0.51 0.8	16	8	20	8	20	20
	bus outputs	6	1.6	48	24	64	24	48	64
Fan-out (LS-loads)									
	standard outputs	10	1 2	40	20	50	20	50	50
	bus outputs	15	4	120	60	160	60	120	160

Table 2: Comparison of HCMOS and LSTTL circuits (V_{CC} = 5 V unless stated otherwise; C_L = 50 pF)

characteristic		74HCXXX (note 1) 74HCTXXX	74LSXXX
Max. quiescent power dissipation over temp. range at V_{CCmax}			
per gate (mW)		0.027	6
per flip-flop (mW)		0.11	22
per 4-stage counter (mW)		0.44	175
per transceiver/buffer (mW)		0.055	60
Max. dynamic power dissipation (C_L = 50 pF)			
at f_i (MHz)	0.1	1 10	0.1 to 1 10
per gate (mW)	0.25	2.25 22	6 22
per flip-flop (mW)	0.35	2.5 24	22 27
per 4-stage counter (mW)	0.70	3 27	175 200
per buffer/transceiver (mW)	0.30	2.5 24	60 90
Operating supply voltage (V)		2 to 6 (HC) 4.5 to 5.5 (HCT)	4.75 to 5.25
Operating temperature range (°C)		−40 to +85 −40 to +125	0 to +70
Max. noise margin (V_{NMH}/V_{NML} V; I_{OHCMOS} = 20 μA; I_{OLSTTL} = 4 mA)		1.4/1.4 (HC) 2.9/0.7 (HCT)	0.7/0.4
Input switching voltage stability over temp. range		±60 mV	±200 mV
Min. output drive current at $T_{amb\ max}$ and V_{CCmin} (mA)			
source current (V_{OH} = 2.7 V; note 2)			
standard logic		−8	−0.4
bus logic		−12	−2.6
sink current			
standard logic (V_{OL} = 0.4 V)		4	4
standard logic (V_{OL} = 0.5 V)		6	8
bus logic (V_{OL} = 0.4 V)		8	12
bus logic (V_{OL} = 0.5 V)		9	24
Typ. output transition time (ns) (C_L = 15 pF)			
standard logic			
t_{TLH}		6	15
t_{THL}		6	6
bus logic			
t_{TLH}		4	15
t_{THL}		4	6
Typ. propagation delay (ns) (C_L = 15 pF; note 3)			
gate t_{PHL}/t_{PLH}		8/8	8/11
flip-flop t_{PLH}		14	15
t_{PHL}		14	22
Typ. clock rate of a flip-flop; note 5 (MHz)		50	33
Max. input current (μA)			
I_{IL}		−1	−400 to −800
I_{IH}		1	40
3-state output leakage current (± μA)		5	20
Reliability (%/1000 h at 60% confidence level)		0.0005	0.008 (note 4)

Notes

1. Data valid for HCMOS between −40 °C and +85 °C.
2. V_{OH} for a few LSTTL bus outputs is specified as 2.4 V.
3. Refer to data sheets for the effect of capacitive loading.
4. RADC report.
5. Measured with a 50% duty factor for HCMOS. For LSTTL, per industry convention, the maximum clock frequency is specified with no constraints on rise and fall times, pulse width or duty factor.

CONSTRUCTION

Our HCMOS family is a result of a continuing development programme to enhance the proven polysilicon-gate CMOS process. Figure 2 shows the construction of a basic inverter from the HE4000B series and its HCMOS successor.

The polysilicon gate of a HCMOS transistor is deposited over a thin gate oxide before the source and drain diffusions are defined. Source and drain regions are formed using ion implantation, with the polysilicon gates acting as masks for the implantation. The source and drain are automatically aligned to the gate, minimizing gate-to-source and gate-to-drain capacitances. In addition, the junction capacitances, which are proportional to the junction area, are reduced because of the shallower diffusions. Figure 3(c) shows the parasitic capacitances in a CMOS inverter.

In a metal-gate CMOS transistor, the source and drain are formed before the gate is deposited. Moreover, the metal gate must overlap the source and drain to allow for alignment tolerances. This is why a metal-gate CMOS transistor has a higher overlap capacitance than an HCMOS transistor. Furthermore, the deeper diffusions of metal-gate CMOS make the junction capacitance larger.

In a silicon-gate MOS transistor, there are three interconnect layers (diffusion, polysilicon and metal) instead of the two layers (diffusion and metal) in a metal-gate MOS transistor. This makes a silicon-gate MOS transistor more compact. The shorter gate length means higher drive capability, which in turn increases the speed at which a silicon-gate MOS transistor can charge or discharge junction capacitance. The drain current of a saturated MOS transistor which determines the speed of the transistor is:

$$I_{DS} = \frac{-\beta}{2} \times \frac{\text{gate width}}{\text{gate length}} \times (\text{gate voltage - threshold voltage})^2$$

where β is the current gain factor which is proportional to the thickness of the oxide layer.

The threshold voltage is typically 0.7 V for HCMOS.

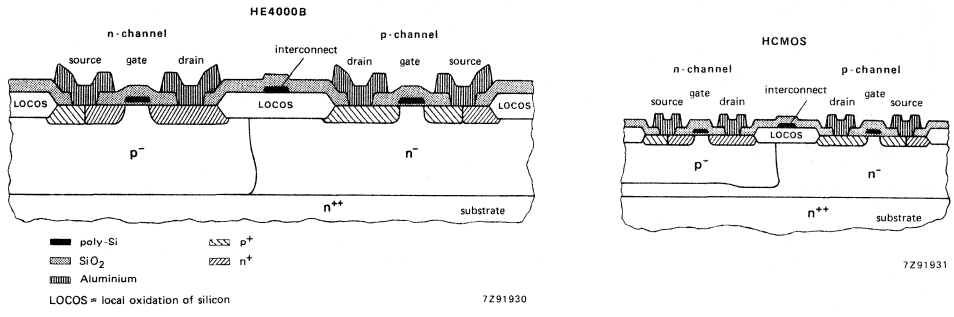


Fig. 2 Basic inverter (left) in HE4000B CMOS, 6 μm gate, and (right) in HCMOS, 3 μm gate.

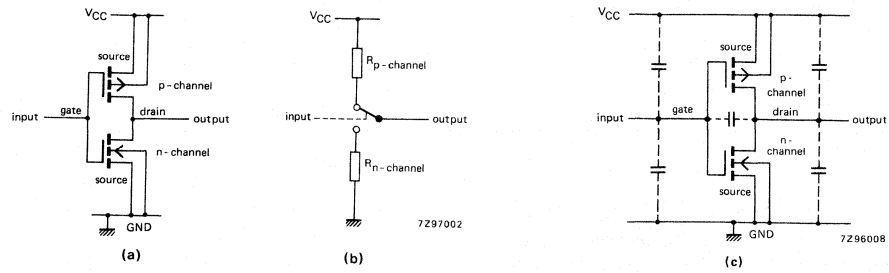


Fig. 3 (a) Basic CMOS inverter; (b) electrical equivalent; (c) parasitic capacitances in a CMOS inverter.

AC CHARACTERISTICS

Test conditions

The propagation delays and transition times specified in the HCMOS data sheets are guaranteed when the circuits are tested according to the conditions stated in the chapter 'Family Characteristics', section 'Family Specifications'. For some circuits such as counters and flip-flops, the test conditions are defined further by the a.c. set-up requirements specified in the data sheet.

Values given in the data sheets are for the whole operating temperature range (−40 to +125 °C) and the supply voltages used are 2.0 V, 4.5 V and 6.0 V for 74HC devices, and 4.5 V for 74HCT devices. This is a much tougher specification than that commonly used for LSTTL, where the characteristics are usually only specified at 25 °C and for a 5 V supply. Furthermore, the published a.c. characteristics of HCMOS are guaranteed for a capacitive test load of 50 pF, a more realistic load than the 15 pF specified for LSTTL and one that loads the device as the output switches. The published values for HCMOS are therefore representative of those measured in actual systems.

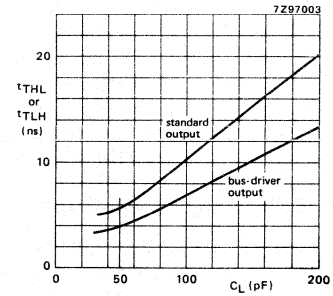
Comparing the speed of HCMOS and LSTTL

A feature of a HCMOS circuit is its speed - in general, comparable to that of its LSTTL equivalent. Owing to the different (more informative) way of specifying data for HCMOS devices, it will be useful to indicate how to compare the published data for HCMOS and LSTTL.

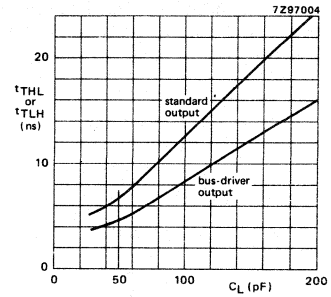
For example, in an LSTTL specification, the use of a 15 pF load instead of a 50 pF one means the maximum propagation delays and enable times published for the LSTTL device will be up to 2.5 ns (typ. 1.3 ns) shorter than those for the HCMOS equivalent. In addition, measuring at the nominal LSTTL supply voltage of 5 V instead of 4.5 V (HCMOS) reduces propagation delays and enable times by a further 10%. So, a 30 ns propagation delay for a HCMOS device is equivalent to a (30 - 2.5)0.9 = 25 ns delay for an LSTTL device measured at 4.5 V and with a 15 pF load.

Disable times are measured under different test conditions too - for HCMOS with a 50 pF, 1 kΩ load, for LSTTL with a 5 pF, 2 kΩ load or for a 45 pF, 667 Ω load. To compare a HCMOS disable time with that for a LSTTL device with a 5 pF load, subtract 4 ns from the published HCMOS disable time and multiply by 0.9. To compare a value for a 45 pF load, subtract 2 ns and multiply by 0.9. For example, a 30 ns HCMOS disable time is equivalent to (30 - 4)0.9 = 23 ns for a 5 pF load and (30 - 2)0.9 = 25 ns for a 45 pF load.

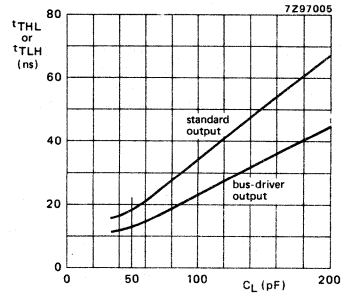
Set-up hold and removal times are not affected by output load, only by supply voltage. To compare a published HCMOS value with an LSTTL value, multiply the HCMOS value by 0.9.



(a) V_{CC} = 6 V



(b) V_{CC} = 4.5 V



(c) V_{CC} = 2 V

Fig. 4 Typical output transition times as a function of load capacitance; T_{amb} = 25 °C; for 74HCT circuits the data at V_{CC} = 4.5 V only is valid.

Operating frequency is also unaffected by output load, but is affected by supply voltage. To compare a published HCMOS value with an LSTTL value, multiply the value for HCMOS at 4.5 V by 1.1.

In general, these guidelines apply both to 74HC and to 74HCT devices. For 74HCT devices however, the propagation delay is the time for the output to reach 1.4 V (compared with 50%V_{CC} for 74HC devices), so HIGH-to-LOW output transition times are slightly more dependent on load and the LOW-to-HIGH transition times are slightly less dependent on load than the 74HC versions.

Propagation delays and transition times

The symmetrical push-pull output structure of both 74HC and 74HCT devices gives symmetrical rise/fall times and provides for a well-balanced system design. Table 3 shows the maximum output transition times for all standard and bus-driver HCMOS outputs.

The influence of capacitive loading on output transitions is shown in Fig.4; A good approximation of the output transition times can be calculated using the data of Table 4.

Table 3: Maximum output transition times (C_L = 50 pF)

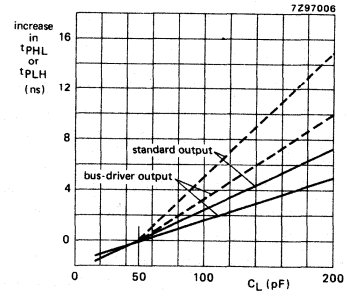
	V_{CC} (V)	maximum output transition time (ns) T_{amb} = 25 °C	T_{amb} = 85 °C	T_{amb} = 125 °C
standard	2	75	95	110
output	4.5*	15	19	22
	6	13	16	19
bus-driver	2	60	75	90
output	4.5*	12	15	18
	6	10	13	15

* 74HC and 74HCT devices; all other data for 74HC devices only.

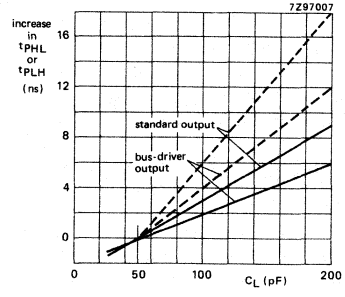
Table 4: Typical output transition times for load capacitances greater than the standard 50 pF load, see Fig.4

V_{CC}	t_{THL} or t_{TLH} standard output	bus-driver output
2.0 V	18.5 ns + 0.32 ns/pF	12.5 ns + 0.22 ns/pF
4.5 V	6.6 ns + 0.12 ns/pF	4.5 ns + 0.077 ns/pF
6.0 V	5.6 ns + 0.10 ns/pF	3.8 ns + 0.065 ns/pF

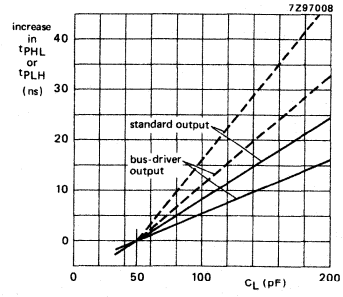
Note: values in pF are the load capacitance minus 50 pF.



(a) V_{CC} = 6 V



(b) V_{CC} = 4.5 V



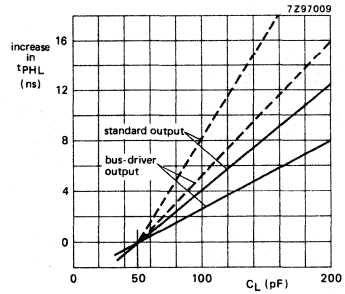
(c) V_{CC} = 2 V

– – – expected maximum

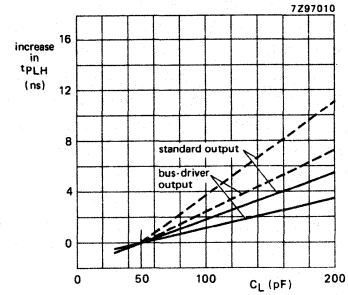
——— typical value

Fig. 5 Increase in propagation delay for 74HC devices as a function of load capacitance; T_{amb} = 25 °C.

A parameter specified for TTL devices is the output short-circuit current HIGH (I_{OS}). Originally intended to reassure the TTL user that the device would withstand accidental grounding, this parameter has become a measure of the ability of the circuit to charge the line capacitance and is used to calculate propagation delays. In CMOS devices however, there is no need to specify I_{OS} because the purely capacitive loads allow extrapolation of the a.c. parameters over the whole loading range. Figure 5 (for 74HC devices) and Fig.6 (for 74HCT devices) show the increase in propagation delay for loads greater than 50 pF. The additional delay can be calculated from the output saturation current (short-circuit current). Referring to the output characteristics (Figs.31 to 34), the propagation delay is the time taken for the output voltage to reach 50% of V_{CC} for 74HC devices, or 1.4 V for 74HCT devices. Since a saturated output transistor acts as a current source, the additional delay is $\Delta CV/I$, where ΔC is the load capacitance minus 50 pF, V is the voltage swing at the output to the switching level of the next circuit, and I is the average source current of the saturated output.



(a) HIGH-to-LOW transition



(b) LOW-to-HIGH transition

— — — expected maximum
——— typical value

Fig. 6 Increase in propagation delay for 74HCT devices as a function of load capacitance; the different values for t_{PHL} and t_{PLH} are due to the asymmetrical reference level of 1.3 V at the outputs; T_{amb} = 25 °C; V_{CC} = 4.5 V.

Supply voltage dependence of propagation delay

The dynamic performance of a CMOS device depends on its drain characteristics. These are related to the switching thresholds and the gate-to-source voltage V_{GS} which is equal to the supply voltage V_{CC}. A reduction in V_{CC} adversely affects the drain characteristics, increasing the propagation delays.

Over the supply voltage range of 74HCT devices, 4.5 V to 5.5 V, the effects of different propagation delays on performance are minimal. Over the supply voltage range of 74HC circuits, 2 to 6 V, the effects on performance are significant, see Figs.7 and 8.

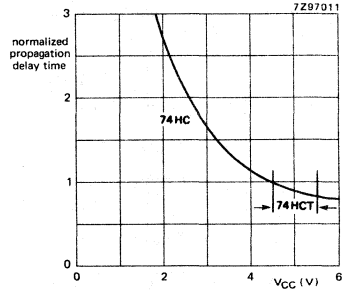


Fig. 7 Propagation delay as a function of supply voltage; T_{amb} = 25 °C; C_L = 50 pF.

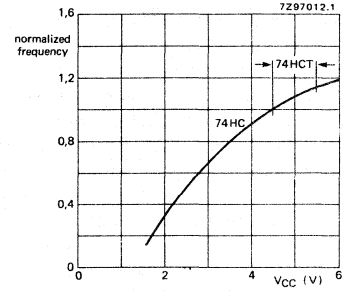


Fig. 8 Operating frequency as a function of supply voltage; T_{amb} = 25 °C; C_L = 50 pF.

Temperature dependence of propagation delay

In TTL circuits, β (current gain), internal resistances and forward-voltage drops are all temperature-dependent. In HCMOS circuits, essentially only the carrier mobility, which affects the propagation delay, is temperature dependent. In general, propagation delay increases by about 0.3% per °C above 25 °C.

Between 25 °C and 125 °C,

$$t_P = t_P'(1.003)^{T_{amb}-25}$$

where:
t_P' is the propagation delay at 25 °C,
T_{amb} is the ambient temperature in °C.

Between −40 °C and +25 °C,

$$t_P = t_P'(0{,}997)^{25-T_{amb}}$$

Figure 9 shows the temperature dependence of a characteristic such as propagation delay.

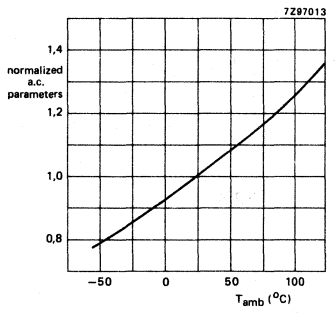


Fig. 9 Typical influence of temperature on a.c. parameters; V_{CC} = 5 V.

Derating system for a.c. characteristics

Because HCMOS devices are a coherent family, manufactured under strictly-controlled conditions, it is possible to have a common set of derating coefficients for temperature and supply voltage that is valid for all a.c. characteristics of all devices. Table 5 shows the derating coefficients which are derived from the published values of the a.c. characteristics at 25 °C for V_{CC} = 4.5 V, denoted by x in the Table. The coefficients have been established after extensive high-temperature testing at many supply voltages. A temperature coefficient of −0.4%/°C was established after comparing the test results with worst-case calculations. The voltage derating given in Table 5 is conservative compared with that shown in Fig.7 for propagation delay. For operating frequencies (Fig.8), the reciprocal of the derating coefficients shown should be used.

Table 5: Derating coefficients for the a.c. characteristics of HCMOS devices

supply voltage	ambient temperature 25 °C	85 °C	125 °C
2 V	5 (5x)	6.25 (5y)	7.5 (5z)
4.5 V*	1 (x)	1.25 (y = 1.25x)	1.5 (z = 1.5x)
6 V	0.85 (0.85x)	1.0625 (0.85y)	1.275 (0.85z)

All coefficients are derived from the value of the a.c. characteristic at V_{CC} = 4.5 V and T_{amb} = 25 °C denoted in the table by x.

* 74HC and 74HCT devices; all other data for 74HC devices only.

Clock pulse requirements

All HCMOS flip-flops and counters contain master-slaves with level-sensitive clock inputs. When the voltage at the clock input reaches the voltage threshold of the device, data in the master (input) section is transferred to the slave (output) section. The threshold for 74HC devices is typically 50% of V_{CC} and that for 74HCT devices is 28% of V_{CC} (1.4 V at V_{CC} = 5 V). The thresholds are virtually independent of temperature.

The use of voltage thresholds for clocking is an improvement over a.c. coupled clock inputs, but it does not make the devices totally insensitive to clock-edge rates. When clocking occurs, the internal gates and output circuits of the device dump current to ground, producing a noise transient that is equal to the algebraic sum of the internal and external ground plane noise. When a number of loaded outputs change simultaneously, the device ground reference (and therefore the clock reference) can rise by as much as 500 mV. If the clock input of a positive-edge triggered device is at or near to its threshold during a noise transient, multiple triggering can occur. To prevent this, the rise and fall times of the clock inputs should be less than the published maximum (500 ns at V_{CC} = 4.5 V).

In the HCMOS family, all the J-K flip-flops have a Schmitt-trigger circuit at the clock input, which eliminates the need to specify a maximum rise/fall time. The flip-flops 74HC/HCT73, 74, 107, 109 and 112 have special Schmitt-trigger circuits for increased tolerance to slow rise/fall times and ground noise.

The published maximum input clock frequency ratings for clocked devices are for a 50% duty factor input clock. At these rated frequencies, the outputs will swing between V_{CC} and GND, assuming no d.c. load on the outputs. This is a very conservative and reliable method of rating the

clock-input-frequency limits for HCMOS devices which are always at least as good as those for LSTLL even though they may appear to be inferior. This is because the maximum operating frequency of a TTL device is published, not for a 50% duty factor clock, but for a minimum clock pulse width.

System (parallel) clocking

In synchronously-clocked systems, spreads in the clock threshold levels of devices can cause logic errors if slow clock edges are used. For example, if data in one circuit changes before the clock threshold of the next sequential circuit is reached, a logic error will occur, see Fig.10.

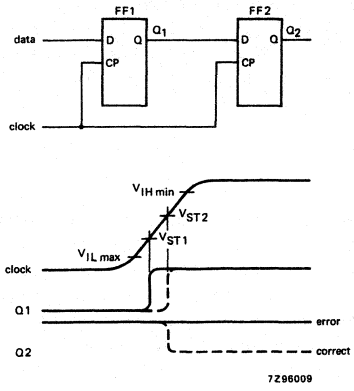


Fig. 10 In synchronously-clocked systems, changing the data in one device before the clock switching threshold of the next has been reached can cause logic errors. V_{ST1} is the clock threshold of device 1; V_{ST2} is the clock threshold of device 2.

To prevent this type of logic error, the maximum rise or fall time of the clock pulse should be less than twice the propagation delay of the flip-flop.

For a HCMOS device, the rise/fall time must be limited to 1000, 500 or 400 ns for V_{CC} = 2 V, 4.5 V and 6 V respectively. If these times are exceeded, noise on the input or power supply rails may cause the outputs to oscillate during transitions, causing logic errors and excessive power dissipation.

Minimum a.c. characteristics

Minimum values of a.c. characteristics are not specified in the data sheets. However, it is sometimes useful to know them, for example when checking whether data set-up and hold times are obeyed. At 25 °C and 4.5 V supply voltage, the minimum values are one quarter of the published maximum values. To calculate the minimum values at other temperatures, derate by 0.27%/°C.

Table 6 gives the derating coefficients for calculating the minimum propagation delays of HCMOS devices at various supply voltages and temperatures.

Table 6: Derating coefficient for the expected minimum propagation delay of HCMOS devices

supply voltage	ambient temperature 25 °C	85 °C	125 °C
2 V	2 (2x)	2.34 (2y)	2.62 (2z)
4.5 V*	1 (x)	1.17 (y = 1.17x)	1.31 (z = 1.31x)
6 V	0.8 (0.8x)	0.936 (0.8y)	1.048 (0.8z)

All coefficients are derived from the value of the a.c. characteristic at V_{CC} = 4.5 V and T_{amb} = 25 °C denoted in the table by x.

* 74HC and 74HCT devices; all other data for 74HC devices only.

POWER DISSIPATION

Static

When a HCMOS device is not switching, the p-channel and n-channel transistors don't conduct at the same time, so leakage current flows between V_{CC} and GND. Because this leakage current is typically a few nA, HCMOS power dissipation is extremely low.

Static power dissipation can be calculated for both 74HC and 74HCT devices from the maximum quiescent current specified in the data sheets, see Table 7.

Table 7: Maximum quiescent current of HCMOS devices at V_{CCmax}* (V_I = V_{CC} or GND; I_O = 0)

device complexity	quiescent current typical at 25 °C	maximum 25 °C	85 °C	125 °C
SSI	2 nA	2 μA	20 μA	40 μA
FF	4 nA	4 μA	40 μA	80 μA
MSI	8 nA	8 μA	80 μA	160 μA

* 6 V for 74HC; 5.5 V for 74HCT.

Dynamic

When a device is clocked, power is dissipated charging and discharging on-chip parasitic and load capacitances. Power is also dissipated at the moment the output switches when both the p-channel and the n-channel transistors are partially conducting. However, this transient energy loss is typically only 10% of that due to parasitic capacitance.

The total dynamic power dissipation per device (P_D) is:

$$P_D = C_{PD}V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) \quad (1)$$

where:

C_{PD} is the power dissipation capacitance per package
f_i is the input frequency
f_o is the output frequency
C_L is the total external load capacitance per output.

The second term of equation (1) implies summing the product of the effective output load capacitance and frequency for each output. However, a good approximation of the total dynamic power dissipation of an HCMOS system can be obtained by summing the published C_{PD} values and load capacitance for the HCMOS devices used and, assuming an average frequency, using equation (1).

For one-shot circuits, gates configured as oscillators, phase-locked loops and devices used in a linear mode, additional dissipation is caused by static supply currents (I_{CC}) whose values are given in the device data sheets.

Power dissipation capacitance

C_{PD} is specified in the device data sheets, the published values being calculated from the results of tests described in this section. The test set-up is shown in Fig.11. The worst-case operating conditions for C_{PD} are always chosen and the maximum number of internal and output circuits are toggled simultaneously, within the constraints listed in the data sheet. Table 8 gives the pin status for HCMOS devices during a C_{PD} test. Devices which can be separated into independent sections are measured per section, the others are measured per device.

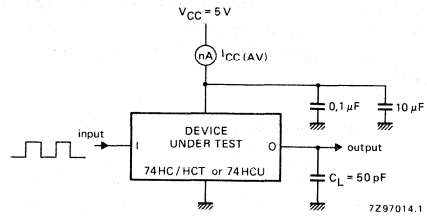


Fig. 11 Test set-up for determining C_{PD}. The input pulse is a square wave between V_{CC} and GND; $t_r = t_f \leqslant 6$ ns; $T_{amb} = 25\,^{\circ}C$. All switching outputs are loaded with 50 pF (including test jig capacitance). Unused inputs are connected to V_{CC} or GND.

The recommended test frequency for determining C_{PD} is 1 MHz, but this is best increased to 10 MHz when I_{CC} is low and the device quiescent current influences $I_{CC(AV)}$. Loading the switched outputs gives a more realistic value of C_{PD}, because it prevents transient 'through-currents' in the output stages. Furthermore, automatic testers often introduce about 30 pF to 40 pF on each device pin.

The values of C_{PD} in the data sheet have been calculated using:

$$C_{PD} = \frac{I_{dyn(device)}}{V_{CC}f_i}$$

where:

$I_{dyn(device)} = I_{CC(AV)} - I_{dyn(load)}$
and
$I_{dyn(load)} = \Sigma(C_L V_{CC} f_o)$

Table 8: Pin conditions for C_{PD} tests.

74HC/HCT	equivalent load (pF)	pin numbers																										
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
00	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
02	50	C	P	L	O	D	D	G	D	D	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
03	0	P	H	B	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
04	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
U04	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
08	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
10	50	P	H	D	D	D	O	G	O	D	D	D	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
11	50	P	H	D	D	D	O	G	O	D	D	D	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
14	50	P	C	D	O	D	O	G	O	D	O	D	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
20	50	P	H	O	H	H	C	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
21	50	P	H	O	H	H	C	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
27	50	P	L	D	D	D	O	G	O	D	D	D	C	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
30	50	P	H	H	H	H	H	G	C	O	O	H	H	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
32	50	P	L	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
42	100	C	C	O	O	O	O	O	G	O	O	O	L	L	L	P	V	–	–	–	–	–	–	–	–	–	–	–	–
58	50	P	D	D	D	D	O	G	O	L	L	L	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
73	50	P	H	H	V	D	D	D	O	O	D	G	C	C	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
74	50	H	Q	P	H	C	C	G	O	O	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
75	50	C	Q	D	D	V	D	D	O	O	O	O	G	P	O	O	C	–	–	–	–	–	–	–	–	–	–	–	–
85	50	L	H	P	H	O	C	O	G	L	L	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
86	50	P	L	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
93	47	Q	L	L	D	V	D	D	C	C	G	C	C	D	P	–	–	–	–	–	–	–	–	–	–	–	–	–	–
107	50	H	C	C	H	O	O	G	D	D	D	D	P	H	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
109	50	H	H	L	P	H	C	C	G	O	O	D	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
112	50	P	H	H	H	C	C	O	G	O	D	D	D	D	D	H	V	–	–	–	–	–	–	–	–	–	–	–	–
123	100	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
125	50	L	P	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
126	50	H	P	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
132	50	P	H	C	D	D	O	G	O	D	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
137	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
138	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
139	100	L	P	L	C	C	O	O	G	O	O	O	O	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
147	50	H	H	H	H	H	O	O	G	C	H	P	H	H	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
151	100	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
153	50	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
154	100	C	C	O	O	O	O	O	O	O	O	O	G	O	O	O	O	O	L	L	L	L	L	P	V	–	–	–	–
157	50	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
158	50	P	L	H	C	L	L	O	G	O	L	L	O	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
160	55	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
161	50	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–

(continued on next page)

Table 8 (continued)

74HC/ HCT	equiv- alent load (pF)	pin numbers																										
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
162	55	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
163	50	H	P	D	D	D	D	H	G	H	H	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
164	200	Q	H	C	C	C	C	G	P	H	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
165	50	H	P	D	D	D	D	C	G	C	Q	D	D	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
166	25	Q	D	D	D	D	L	P	G	H	D	D	D	C	D	H	V	–	–	–	–	–	–	–	–	–	–	–	–
173	25	L	L	C	O	O	O	P	G	L	L	D	D	D	Q	L	V	–	–	–	–	–	–	–	–	–	–	–	–
174	25	H	C	Q	D	O	D	O	G	P	O	D	O	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–
175	50	H	C	C	Q	D	O	O	G	P	O	O	D	D	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
181	250	P	H	H	L	L	H	H	L	C	C	C	G	C	B	C	C	C	L	H	L	H	L	H	V	–	–	–	–
182	150	H	L	H	L	H	L	O	G	C	O	C	C	P	H	L	V	–	–	–	–	–	–	–	–	–	–	–	–
190	60	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
191	53	D	C	C	L	L	C	C	G	D	D	H	C	C	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
192	60	D	C	C	H	P	C	C	G	D	D	H	C	C	L	D	V	–	–	–	–	–	–	–	–	–	–	–	–
193	50	D	C	C	H	P	C	C	G	D	D	H	C	C	L	D	V	–	–	–	–	–	–	–	–	–	–	–	–
194	100	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
195	125	H	H	L	D	D	D	D	G	H	P	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
221	100	L	H	P	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
237	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
238	100	P	L	L	L	L	H	O	G	O	O	O	O	O	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
240	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	D	V	–	–	–	–	–	–	–	–
241	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	H	V	–	–	–	–	–	–	–	–
242	50	L	O	P	D	D	D	G	O	O	O	C	O	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
243	50	L	O	P	D	D	D	G	O	O	O	C	O	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
244	50	L	P	O	D	O	D	O	D	O	G	D	O	D	O	D	O	D	C	D	V	–	–	–	–	–	–	–	–
245	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
251	100	D	D	L	H	C	C	L	G	L	L	P	D	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
253B	50	L	L	D	D	L	H	C	G	O	D	D	D	D	P	D	V	–	–	–	–	–	–	–	–	–	–	–	–
257	50	P	L	H	C	D	D	O	G	O	D	D	O	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
258	50	P	L	H	C	D	D	O	G	O	D	D	O	D	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
259	25	L	L	L	C	O	O	O	G	O	O	O	O	Q	P	H	V	–	–	–	–	–	–	–	–	–	–	–	–
7266	50	P	L	C	O	D	D	G	D	D	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
273	25	H	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
280	100	L	L	O	L	C	C	G	P	L	L	L	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
283	250	C	H	L	C	P	H	L	G	C	C	H	L	C	L	H	V	–	–	–	–	–	–	–	–	–	–	–	–
297	12	H	H	H	P	Q	L	C	G	D	D	O	O	D	H	H	V	–	–	–	–	–	–	–	–	–	–	–	–
299	250	H	L	L	C	C	C	C	C	H	G	Q	P	C	C	C	C	C	D	L	V	–	–	–	–	–	–	–	–
354	100	D	D	D	D	D	D	L	H	L	G	L	L	L	P	L	L	H	C	C	V	–	–	–	–	–	–	–	–
356	50	D	D	D	D	D	D	D	Q	P	G	L	L	L	L	L	L	H	C	C	V	–	–	–	–	–	–	–	–
365	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
366	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–

(continued on next page)

Table 8 (continued)

74HC/ HCT	equiv-alent load (pF)	pin numbers																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
367	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
368	50	L	P	C	D	O	D	O	G	O	D	O	D	O	D	L	V	–	–	–	–	–	–	–	–	–	–	–	–
373	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
374	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
377	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
390	50	P	L	C	Q	C	C	C	G	O	O	O	D	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
393	47	P	L	C	C	C	C	G	O	O	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
423	100	L	P	H	C	O	O	O	G	D	D	D	O	C	O	R	V	–	–	–	–	–	–	–	–	–	–	–	–
533	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
534	25	L	C	Q	D	O	O	D	D	O	G	P	O	D	D	O	O	D	D	O	V	–	–	–	–	–	–	–	–
540	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
541	50	L	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
563	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
564	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
573	25	L	P	D	D	D	D	D	D	D	G	H	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
574	25	L	Q	D	D	D	D	D	D	D	G	P	O	O	O	O	O	O	O	C	V	–	–	–	–	–	–	–	–
583	250	H	H	H	L	L	C	C	G	C	C	C	H	P	L	L	V	–	–	–	–	–	–	–	–	–	–	–	–
597	25	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	–	–	–	–	–	–	–	–	–	–	–	–
7597	25	D	D	D	D	D	D	D	D	G	C	H	P	D	H	Q	D	V	–	–	–	–	–	–	–	–	–	–	–
640	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
643	50	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	V	–	–	–	–	–	–	–	–
646	50	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
648	50	D	L	H	P	D	D	D	D	D	D	D	G	O	O	O	O	O	O	O	C	L	D	D	V	–	–	–	–
670	100	Q	Q	Q	L	P	C	C	G	C	C	L	L	L	P	Q	V	–	–	–	–	–	–	–	–	–	–	–	–
688	50	L	P	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	L	C	V	–	–	–	–	–	–	–	–
4002	50	C	P	L	L	L	O	G	O	D	D	D	D	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4015	100	P	C	O	O	O	D	D	G	D	O	C	C	C	L	Q	V	–	–	–	–	–	–	–	–	–	–	–	–
4016	0	O	O	O	O	D	D	G	O	O	O	O	D	P	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4017	55	C	C	C	C	C	C	C	G	C	C	C	C	L	P	L	V	–	–	–	–	–	–	–	–	–	–	–	–
4020	48	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
4024	48	P	L	C	C	C	C	G	O	C	O	C	C	O	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4040	48	C	C	C	C	C	C	C	G	C	P	L	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
4046A	50	O	C	L	O	H	O	O	G	O	O	O	O	O	P	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4049	50	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	O	–	–	–	–	–	–	–	–	–	–	–	–
4050	50	V	C	P	O	D	O	D	G	D	O	D	O	O	D	O	O	–	–	–	–	–	–	–	–	–	–	–	–
4051	0	O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4052	0	O	O	O	O	O	L	G	G	L	P	O	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4053	0	O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	–	–	–	–	–	–	–	–	–	–	–	–
4059	17	P	D	H	L	L	L	L	L	L	L	H	G	H	H	L	L	L	L	L	L	L	L	C	V	–	–	–	–
4060	106	C	C	C	C	C	C	C	G	C	C	P	L	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–

(continued on next page)

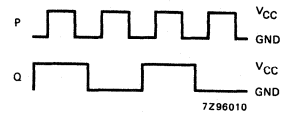
Table 8 (continued)

74HC/ HCT	equiv-alent load (pF)	pin numbers																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
4066	0	O	O	O	O	D	D	G	O	O	O	O	D	P	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4067	0	O	O	O	O	O	O	O	O	O	P	L	G	L	L	L	O	O	O	O	O	O	O	O	V	–	–	–	–
4075	50	P	L	D	D	D	O	G	L	C	O	D	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4094	250	H	Q	P	C	C	C	C	G	C	C	C	C	C	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–
4316	0	O	O	O	O	P	D	L	G	G	O	O	O	O	D	D	V	–	–	–	–	–	–	–	–	–	–	–	–
4351	0	O	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	–	–	–	–	–	–	–	–
4352	0	O	O	O	O	O	O	L	H	G	G	H	P	L	O	O	O	O	O	O	V	–	–	–	–	–	–	–	–
4353	0	O	O	O	O	O	O	L	H	G	G	H	P	L	O	L	O	O	O	O	V	–	–	–	–	–	–	–	–
4510	55	L	C	D	D	L	C	C	G	L	H	C	D	D	C	P	V	–	–	–	–	–	–	–	–	–	–	–	–
4511	200	L	L	H	H	L	L	P	G	C	C	O	O	C	O	C	V	–	–	–	–	–	–	–	–	–	–	–	–
4514	100	H	P	L	O	O	O	O	O	C	O	C	G	O	O	O	O	O	O	O	O	L	L	L	V	–	–	–	–
4515	100	H	P	L	O	O	O	O	O	C	O	C	G	O	O	O	O	O	O	O	O	L	L	L	V	–	–	–	–
4516	50	L	C	D	D	L	C	C	G	L	H	C	D	D	C	P	V	–	–	–	–	–	–	–	–	–	–	–	–
4518	50	P	H	C	C	C	C	L	G	D	D	O	O	O	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–
4520	47	P	H	C	C	C	C	L	G	D	D	O	O	O	O	D	V	–	–	–	–	–	–	–	–	–	–	–	–
4538	100	G	R	H	P	H	C	C	G	O	O	D	D	L	O	G	V	–	–	–	–	–	–	–	–	–	–	–	–
4543	50	H	L	L	H	L	P	L	G	C	C	C	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
7030	325	G	G	C	P	Q	Q	Q	Q	Q	Q	Q	Q	Q	G	L	C	C	C	C	C	C	C	C	C	C	P	H	V
7046A	50	O	C	L	O	H	O	O	G	O	O	O	O	O	P	O	V	–	–	–	–	–	–	–	–	–	–	–	–
40102	5	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–
40103	3	P	H	L	L	L	L	L	G	H	L	L	L	L	C	H	V	–	–	–	–	–	–	–	–	–	–	–	–
40104	100	H	Q	D	D	D	D	D	G	H	L	P	C	C	C	C	V	–	–	–	–	–	–	–	–	–	–	–	–
40105	200	L	C	P	Q	Q	Q	Q	G	L	C	C	C	C	C	P	V	–	–	–	–	–	–	–	–	–	–	–	–

Key

V = V_{CC} (+5 V)
G = ground
H = logic 1 (V_{CC}) – inputs at V_{CC} for HC types; 3.5 V for HCT types
L = logic 0 (ground)
D = don't care – either H or L but not switching
C = a 50 pF load to ground
O = an open pin; 50 pF to ground is allowed
P = input pulse (see illustration)
Q = half frequency pulse (see illustration)
R = 1 kΩ pull-up resistor to an additional 5 V supply other than the V_{CC} supply
B = both R and C

Input pulses



Conditions for C_{PD} tests

Gates. All inputs except one are held at either V_{CC} or GND, depending on which state causes the output to toggle. The remaining input is toggled at a known frequency. C_{PD} is specified per-gate.

Decoders. One input is toggled, causing the outputs to toggle at the same rate (normally one of the address-select pins is switched while the decoder is enabled). All other inputs are tied to V_{CC} or GND, whichever enables operation. C_{PD} is specified per-independent-decoder.

Multiplexers. One data input is tied HIGH and the other is tied LOW. The address-select and enable inputs are configured such that toggling one address input selects the two data inputs alternately, causing the outputs to toggle. With three-state multiplexers, C_{PD} is specified per output function for enabled outputs.

Bilateral switches. The switch inputs and outputs are open-circuit. With the enable input active, one of the select inputs is toggled, the others are tied HIGH or LOW. C_{PD} is specified per switch.

Three-state buffers and transceivers. C_{PD} is specified per buffer with the outputs enabled. Measurement is as for simple gates.

Latches. The device is clocked and data is toggled on alternate clock pulses. Other preset or clear inputs are held so that output toggling is enabled. If the device has common-locking latches, one latch is toggled by the clock. Three-state latches are measured with their outputs enabled. C_{PD} is specified per-latch.

Flip-flops. Measurement is performed as for latches. The inputs to the device are toggled and any preset or clear inputs are held inactive.

Shift registers. The register is clocked and the serial data input is toggled at alternate clock pulses (as described for latches). Clear and load inputs are held inactive and parallel data are held at V_{CC} or GND. Three-state devices are measured with outputs enabled. If the device is for parallel loading only, it is loaded with 101010..., clocked to shift the data out and then reloaded.

Counters. A signal is applied to the clock input but other clear or load inputs are held inactive. Separate values for C_{PD} are given for each counter in the device.

Arithmetic circuits. Adders, magnitude comparators, encoders, parity generators, ALUs and miscellaneous circuits are exercised to obtain the maximum number of simultaneously toggling outputs when toggling only one or two inputs.

Display drivers. C_{PD} is not normally required for LED drivers because LEDs consume so much power as to make the effect of C_{PD} negligible. Moreover, when blanked, the drivers are rarely driven at significant speeds. When it is needed, C_{PD} is measured with outputs enabled and disabled while toggling between lamp test and blank (if provided), or between a display of numbers 6 and 7.

LCD drivers are tested by toggling the phase inputs that control the segment and backplane waveforms outputs.

If either type of driver (LCD or LED) has latched inputs, then the latches are set to a flow-through mode.

One-shot circuits. In some cases, when the device I_{CC} is significant, C_{PD} is not specified. When it is specified, C_{PD} is measured by toggling one trigger input to make the output a squarewave. The timing resistor is tied to a separate supply (equal to V_{CC}) to eliminate its power contribution.

Additional power dissipation in 74HCT devices

When the inputs of a 74HCT device are driven by a TTL device at the specified minimum HIGH output level of $V_{OH} = 2.4$ V, the input stage p-channel transistor does not completely switch off and there is an additional quiescent supply current (ΔI_{CC}). This current has been considerably reduced by proprietary development of 74HCT input stages, see '74HCT inputs'.

The value of ΔI_{CC} specified in the data sheets is per input and at the worst-case input voltage of V_{CC}-2.1 V for V_{CC} between 4.5 and 5.5 V. The value of 2.1 V is the maximum voltage drop across a TTL output HIGH (minimum V_{CC} and minimum V_{OH}), see Table 9.

The additional power dissipation P is:

$P = V_{CC} \times \Delta I_{CC} \times$ duty factor HIGH x unit load coefficient

The unit load coefficient for an input is a factor by which the value of ΔI_{CC} given in the data sheet has to be multiplied. A unit load coefficient is published for each 74HCT device. It is a function of the size of the input p-channel transistor.

Table 9: Worst-case additional quiescent supply current (ΔI_{CC}) for 74HCT devices

	T_{amb} (°C)				UNIT	TEST CONDITIONS		
	74HCT							
	+25		−40 to +85	−40 to +125		V_{CC} V	V_I	OTHER
	typ.	max.	max.	max.				
ΔI_{CC} per input pin for a unit load coefficient of 1*	100	360	450	490	μA	4.5 to 5.5	V_{CC}−2.1 V	other inputs at V_{CC} or GND I_O = 0

* The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case (V_I = 2.4 V; V_{CC} = 5.5 V) specification is: ΔI_{CC} = 0.65 mA (typical) and 1.8 mA (maximum) across temperature.

Power dissipation due to slow input rise/fall times

When an output stage switches, there is a brief period when both output transistors conduct. The resulting 'through-current' is additional to the normal supply current and causes power dissipation to increase linearly with the input rise or fall time.

As long as the input voltage is less than the n-channel transistor threshold voltage, or is higher than V_{CC} minus the p-channel transistor threshold voltage, one of the input transistors is always off and there is no through-current.

When the input voltage equals the n-channel transistor threshold voltage (typ. 0.7 V), the n-channel transistor starts to conduct and through-current flows, reaching a maximum at $V_I = 0.5\,V_{CC}$ for 74HC devices, and $V_I = 28\%V_{CC}$ for 74HCT devices, the maximum current being determined by the geometry of the input transistors. The through-current is proportional to $V_{CC}{}^n$ where n is about 2.2. The supply current for a typical HCMOS input is shown as a function of input voltage transient in Fig.12.

When Schmitt triggers are used to square pulses with long rise/fall times, through-current at the Schmitt-trigger inputs will increase the power dissipation, see Schmitt-trigger data sheets. In the case of RC oscillators, or oscillators constructed with Schmitt triggers this contribution to the power dissipation is frequency-dependent.

Comparison with LSTTL power dissipation

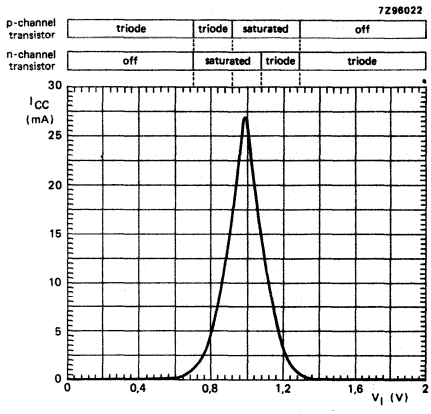
The dynamic power dissipation of a HCMOS device is frequency-dependent; above 1 MHz, that of an LSTTL device is too. Below 1 MHz, the dynamic component of power dissipation of an LSTTL device is negligible compared to the static component. Figure 13 shows the average power dissipation of four HCMOS devices and their LSTTL equivalents. Because all functions in a multi-functional LSTTL device are biased when power is applied, for comparison, the dissipation of whole HCMOS devices besides individual functions are given.

In Fig.13 it can be seen that:

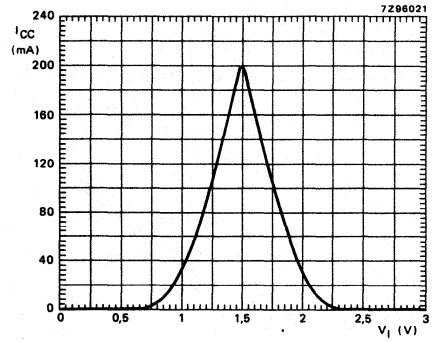
- for SSI gate types, the HCMOS power dissipation is less than LSTTL power dissipation below about 1 MHz
- for more complex types such as a 74HC/HCT138 3-to-8 line decoder HCMOS power dissipation is less than LSTTL power dissipation up to 10 MHz.

In typical microcomputer systems, the operating frequency or the data/address signal rates will usually vary, whereas Fig.13 is for continuous operation at a constant frequency. Average operating frequencies are usually far below the peak frequencies, particularly in the 100 kHz region where the power dissipation of HCMOS is several orders of magnitude less than that of LSTTL.

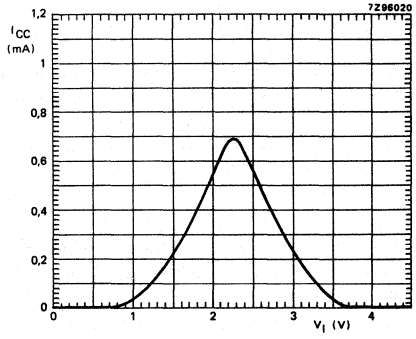
For further information, see chapter 'Power dissipation'.



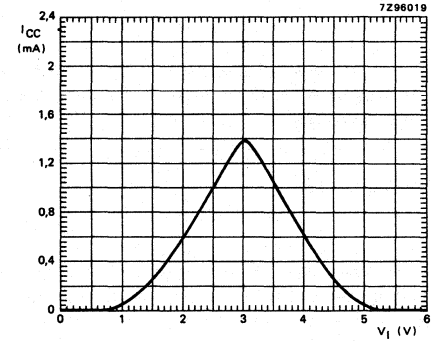
(a) V_{CC} = 2 V



(b) V_{CC} = 3 V



(c) V_{CC} = 4.5 V



(d) V_{CC} = 6 V

Fig. 12 Typical d.c. supply current as a function of input voltage for 74HC circuits; normalized curves for a unit load coefficient of 1. The I_{CC} for a specific 74HC circuit can be calculated by multiplying the values of I_{CC} shown by the unit load coefficient for the 74HCT type given in the data sheet.

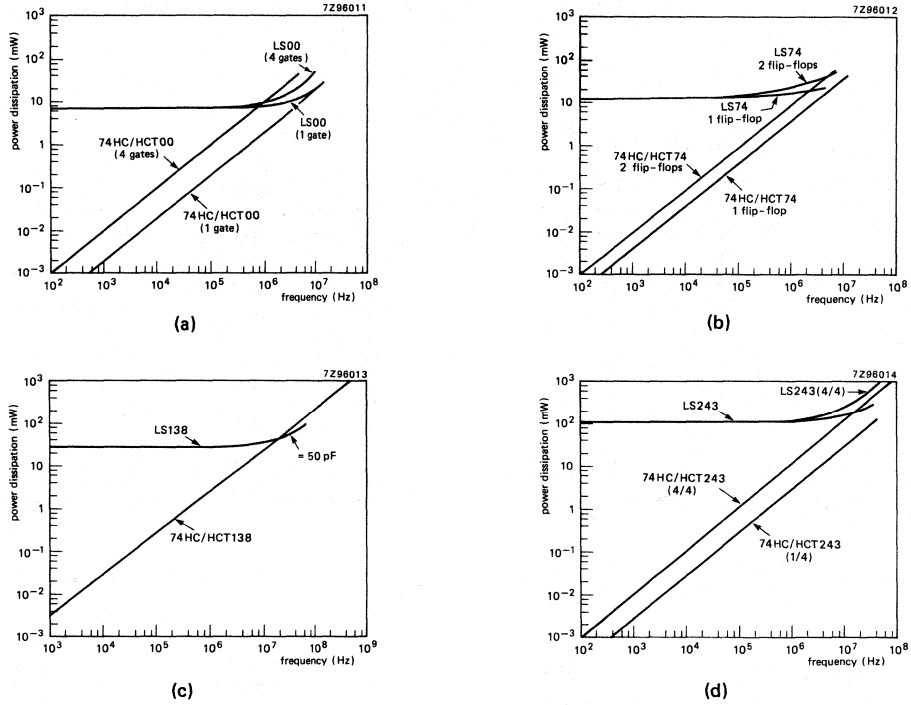


Fig. 13 Typical power dissipation as a function of operating frequency for a variety of LSTTL and HCMOS circuits; (a) quad 2-input NAND gate, (b) dual D-type flip-flop, (c) 3-to-8 line decoder/demultiplexer; inverting, (d) quad 3-state bus transceiver.

SUPPLY VOLTAGE

Range

The supply voltage range of 74HC devices is 2 V to 6 V (Fig.14). This ensures continued use of HCMOS with future generations of memory and microcomputer requiring supply voltages of less than 5 V, simplifies the regulation requirements of power supplies, facilitates battery operation and allows lithium battery back-up. When 74HC devices are used in linear applications, for example when they are used as RC oscillators, a supply of at least 3 V is recommended to ensure sufficient margin for operation in the linear region.

74HCT devices are pin-compatible with LSTTL circuits and are intended as power-saving replacements for them. The 74HCT devices will operate from the traditional 5 V LSTTL supply, but the voltage range is extended to ±10% for both LSTTL temperature ranges (−40 to +85 °C and −40 to +125 °C). This allows extended temperature range LSTTL devices to be replaced by 74HCT devices.

The absolute maximum supply or ground current per pin is ±50 mA for devices with standard output drive, and ±70 mA for devices with bus driver outputs. These currents are only drawn when the outputs of a device are heavily loaded. The average dynamic current at very high frequencies can be calculated using C_{PD}.

The maximum rated supply voltage of HCMOS devices is 7 V and any voltage above this may destroy the device, even though the on-chip parasitic diode break-down voltage is at least 20 V and the threshold voltage of parasitic thick-field oxide transistors is 15 V.

The V_{CC} and GND potentials must never be reversed as this can cause excessive currents to flow through the input protection diodes.

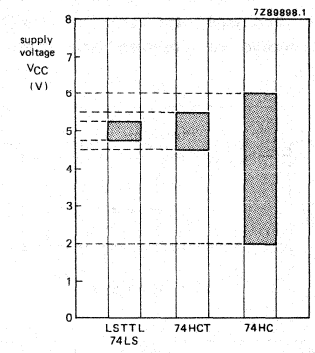


Fig. 14 Supply voltage ranges for LSTTL and HCMOS circuits. The supply voltage range for 74HCT circuits retain the LSTTL nominal supply of 5 V, but the range has been extended from ±5% to ±10% for both the standard and the extended temperature range. 74HC circuits operate with a supply voltage as low as 2 V.

Battery back-up

A battery back-up for a 74HC system is extremely simple. Figure 15 shows an example. The minimum battery voltage required is only 2 V plus one diode drop.

In the example, HIGH-to-LOW level shifters (74HC4049 or 74HC4050) prevent positive input currents into the system due to input signals greater than one diode drop above V_{CC}. If the circuit is such that input voltages can exceed V_{CC}, external resistors should be included to limit the input current to 15 mA for one input (7.5 mA per input for two inputs, 5 mA per input for three inputs, etc.).

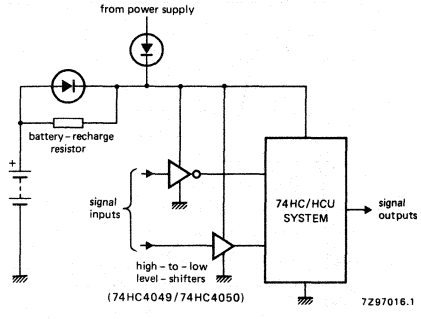


Fig. 15 An HCMOS system with battery back-up.

External resistors may also be necessary in the output circuits to limit the current to 20 mA if the output can be pulled above V_{CC} or below GND. These current limits are set by the parasitic V_{CC}/GND diodes present in all outputs, including three-state outputs.

For further information, see chapter 'Battery back-up.

Power supply regulation and decoupling

The wide power supply range of 2 V to 6 V may suggest that voltage regulation is unnecessary. However, a changing supply voltage will affect system speed, noise immunity and power consumption. Noise immunity, and even the operation of the circuit, can be affected by spikes on the supply lines, so matched decoupling is always necessary in dynamic systems.

Both 74HC and 74HCT devices have the same power supply regulation and decoupling requirements. The best method of minimizing spikes on the supply lines is simple enough – use a good power supply, provide good ground bussing and low a.c. impedances from the V_{CC} and GND pins of each device. The minimum decoupling capacitance depends on the voltage spikes that can be tolerated, which in general should be limited to 400 mV. A local voltage regulator on a printed circuit board can be decoupled using an electrolytic capacitor of 10 to 50 μF. Localized decoupling of devices can be provided by 22 nF per every two to five packages and a 1 μF tantalum capacitor for every ten packages. The V_{CC} line of bus driver circuits and level-sensitive devices can be decoupled from instantaneous loads by a 22 nF ceramic capacitor connected as close to the package as possible.

For further information, see chapter 'Power supply decoupling'.

INPUT/OUTPUT PROTECTION

The gate input of a MOS transistor acts as a capacitor (<1 pF) with very low leakage current (<1 pA). Without protection, such an input could be electrostatically charged to a high voltage that would breakdown the dielectric and permanently damage the device.

The integration process of the HCMOS family allows polysilicon resistors to be formed at all inputs to slow down fast input transients caused by electrostatic discharge and to dissipate some of their energy. These resistors also ensure that the input impedance of an HCMOS device is typically 100 Ω under all biasing conditions, even when V_{CC} is short-circuited to GND – an improvement over direct input diode clamps during power-up.

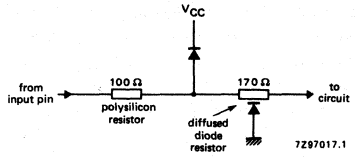


Fig. 16 Standard input protection of 74HC/HCT/HCU inputs against electrostatic discharge.

The standard input protection comprises a series polysilicon resistor and two stages of diode clamping (Fig.16). The typical forward voltage of the diodes is 0.9 V at 2 mA and the reverse breakdown voltage is 20 V. In some applications such as oscillators, the diodes conduct during normal operation, in which case the input current should be limited. The maximum positive input current $+I_{IK}$ per input is 20 mA. For devices with a standard output, the total positive input current is 50 mA; for devices with a bus-driver output, the total input current is 70 mA. The maximum negative input current $-I_{IK}$ per pin is:

14 mA for one input
9 mA for two inputs
6 mA for three inputs
5 mA for four inputs
4 mA for five inputs
3 mA for six to eight inputs.

High-to-low level shifters 74HC4049 and 74HC4050 have a single-sided input protection network (Fig.17) which protects against electrostatic input voltages. The diode D1 is the parasitic drain-to-GND diode of the thick field oxide protection device.

All input pins can withstand discharge voltages up to 2.5 kV (typ.) when tested according to MIL-STD-883B, method 3015, see Fig.18. The output configurations of standard, bus driver, three-state, open drain and I/O ports can withstand >3.5 kV (typ.) because of the large diodes formed by the drain surfaces of the output transistors.

Fig.19 shows the voltage pulse for the discharge test. The rise time t_r prescribed by MIL-STD-883B is ⩽15 ns, but in practice it is helpful to adjust the test set-up to give a rise time of 13±2 ns to avoid correlation problems.

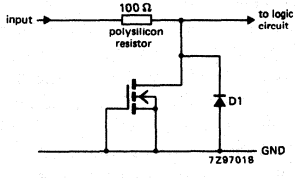
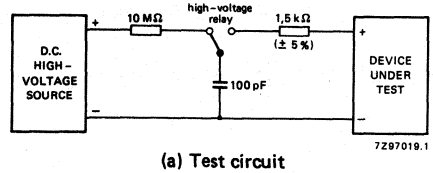


Fig. 17 Input protection of 74HC4049 and 74HC4050.

Although all inputs and outputs are protected against electrostatic discharge, the standard CMOS handling precautions should be observed (see chapter 'Handling precautions').



(a) Test circuit

mode	device under test +	−
1	input	GND
2	GND	input
3	input	V_{CC}
4	V_{CC}	input
5	output	GND
6	GND	output
7	output	V_{CC}
8	V_{CC}	output
9	input	output
10	output	input
11	V_{CC}	GND
12	GND	V_{CC}

all other pins should be left open circuit

(b) Test modes

Fig. 18 Electrostatic discharge test.

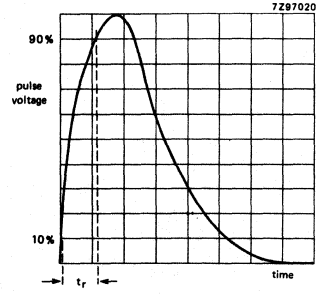


Fig. 19 Test voltage for electrostatic discharge test.

INPUT CIRCUITS

74HC inputs

The 74HC input circuit (Fig.20) includes the resistor/diode network for electrostatic discharge protection and clamps input voltages greater than V_{CC} or less than GND. The circuit is intended for a.c. working and cannot handle heavy d.c. currents for long periods; the maximum input diode current is 20 mA.

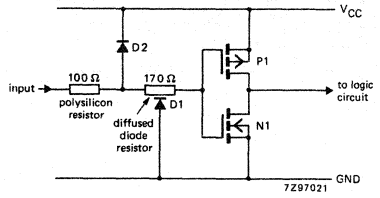


Fig. 20 74HC input circuit.

The 74HC input circuit has no active input current; the only current flowing is through the reversed-biased diodes D1 and D2, typically a few nA reaching a maximum when $V_I = V_{CC}$ or GND.

The MOS transistors P1 (p-channel) and N1 (n-channel) have the same conductance when switched on, giving a typical switching threshold of 50% V_{CC}, see Fig.21. This threshold is almost independent of temperature, a ±60 mV variation of the switching point from −40 to +125 °C being typical. The temperature dependence of V_{IL} is −0.6 mV/°C, that of V_{IH} is +0.6 mV/°C. The only other factors that affect the switching threshold are the spreads of β and V_T of P1 and N1 between devices.

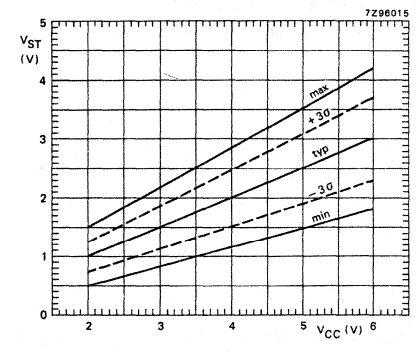


Fig. 21 74HC input switching level as a function of supply voltage.

There is no current path from V_{CC} to GND when the input is lower than V_{TN}, or higher than $V_{CC}-V_{TP}$. However, when the input voltage is in the linear region, a static current path from V_{CC} or GND flows in the input stage (Fig.12). This current is negligible under normal operating conditions when the input rise time $t_r \leqslant 15$ ns, but the power dissipation should be taken into account for devices operating in the linear region. Owing to the voltage gain of the input stage, there is no static flow-through current in the second and subsequent stages. Small currents do flow in these stages during operation when both n-channel and p-channel transistors conduct for brief periods and their effect is included in the C_{PD} value in the data sheets.

74HCT inputs

The 74HCT input stage is similar to that of a 74HC device. It has the same characteristics for LSTTL levels as a 74HC input has for CMOS levels, so there is no trade-off in speed or power dissipation. The switching threshold is lower, 1.4 V at V_{CC} = 5 V. In addition, the 74HCT input circuit, shown in Fig.22, has an enlarged n-channel transistor (N1) and a level-shift diode (D3) has been added. The natural drain voltage of the p-channel transistor (P1) is approximately $V_{CC}-0.6$ V, but when the input voltage is LOW, an auxiliary pull-up transistor (P2) raises this to V_{CC}, cutting off p-channel transistor P3 completely. The input stage is well matched to the load presented by the second stage so that symmetrical propagation delays are obtained.

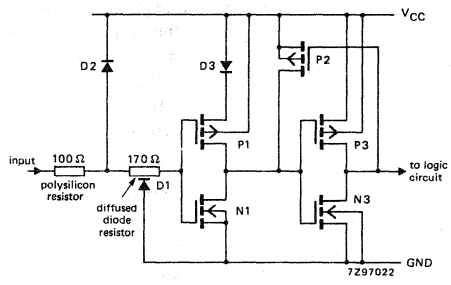


Fig. 22 74HCT input circuit.

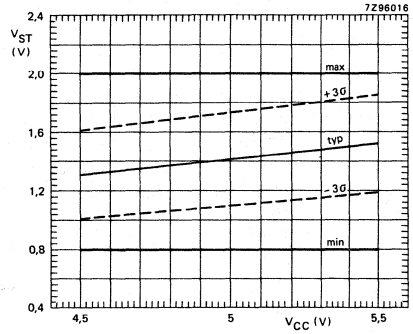


Fig. 23 74HCT input switching level as a function of supply voltage.

Figure 23 shows the switching level as a function of supply voltage.

A TTL HIGH level can be as low as 2.4 V. An input of this order to a HCMOS device would not cut off P1 completely, and additional supply current would flow through the input stage. A level-shift diode D3 and the influence of the back-gate (substrate) connection to P1 minimizes power dissipation caused by this through-current and gives an input switching level compatible with LSTTL. Figure 24 shows the input stage through-current with and without the diode circuit. The peak in the curve occurs at the input switching threshold.

The input stage through-current is virtually zero for a typical TTL HIGH level input of 3.5 V. Thus, this unique 74HCT input structure gives true CMOS low power-consumption when driven by TTL. Typical and maximum through-currents ΔI_{CC} per input are given in the data sheets.

In a system where 74HCT devices are only driven by LSTTL devices, $V_{OH\,min}$ can be 2.7 V except for some bus drivers. With $V_{OH} = 2.7$ V, ΔI_{CC} is half the published value.

Maximum input rise/fall times

All digital circuits can oscillate or trigger prematurely when input rise and fall times are very long. When the input signal to a device is at or near the switching threshold, noise on the line will be amplified and can cause oscillation which, if the frequency is low enough, can cause subsequent stages to switch and give erroneous results. For this reason, Schmitt-triggers are recommended if rise/fall times are likely to exceed 500 ns at $V_{CC} = 4.5$ V.

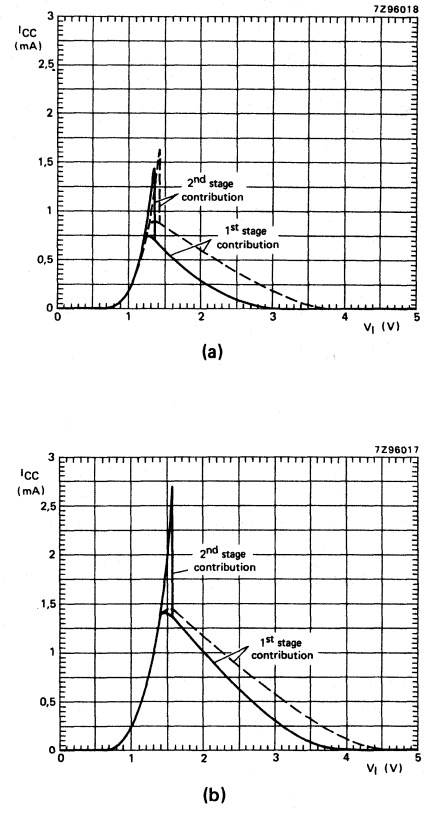


Fig. 24 Additional quiescent supply current ΔI_{CC} (typ.) per input pin of a 74HCT device as a function of supply voltage (unit load coefficient is 1); (a) $V_{CC} = 4.5$ V, (b) $V_{CC} = 5.5$ V.

The flip-flops 74HC/HCT73, 74, 107, 109 and 112 incorporate Schmitt-trigger input circuits and the 74HC/HCT14 and 132 are dedicated Schmitt triggers with specified input levels.

For further information, see chapter 'Schmitt trigger applications'.

Termination of unused inputs

To prevent any possibility of linear operation of the input circuitry of an LSTTL device, it is good practice to terminate all unused LSTTL inputs to V_{CC} via a 1.2 kΩ resistor. Inputs should not be connected directly to GND or V_{CC}, and they should not be left floating.

Unlike LSTTL inputs, the impedance of 74HC and 74HCT inputs is very high and unused inputs must be terminated to prevent the input circuitry floating into the linear mode of operation which would increase the power dissipation and could cause oscillation. Unused 74HC and 74HCT inputs should be connected to V_{CC} or GND, either directly (a distinct advantage over LSTTL), or via resistors of between 1 kΩ and 1 MΩ. Since the resistors used to terminate the inputs of LSTTL devices are usually between 220 Ω and 1.2 kΩ, it is often possible to directly replace LSTTL circuits with their 74HCT counterparts.

Some of the bidirectional (transceiver) logic devices in the HCMOS family have common I/O pins. These pins cannot be connected directly to V_{CC} or GND. Instead, when defined as inputs, they should be connected via a 10 kΩ resistor to V_{CC} or GND.

Input current

Figure 25 shows the typical input leakage current of a HCMOS device as a function of ambient temperature for a V_{CC} of 6 V. Over the total operating temperature range, the input leakage current is well below the rating specified in the JEDEC standard (100 nA between −55 °C and +25 °C and 1 μA at +85 °C and +125 °C. The reason for this difference between the measured performance and the rating is the high-speed testing limitations associated with test system resolution and the measurement of settling time. A secondary reason is that the rating is end-of-line, allowing some leakage current shift due to the ingress of moisture or foreign material.

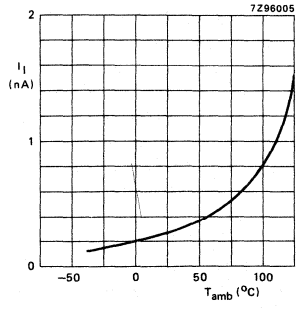


Fig. 25 Typical HCMOS input leakage current I_I as a function of ambient temperature T_{amb}.

Input capacitance

Since CMOS inputs present essentially no load, fan-out is limited only by the input capacitance. This is specified as 3.5 pF (typ.) and comprises package, bonding pad/interconnecting track, input protection diode and transistor gate capacitances. Figs.26 and 27 show the typical input capacitances for powered 74HC and 74HCT devices. The initial decrease in capacitance as V_I rises from zero or falls from 5 V is due to increased reverse bias on the protection diodes. The peak is caused by internal Miller feedback capacitance when the inverter is in its linear mode. A conservative value for the maximum input capacitance is 10 pF (20 pF for I/O pins owing to the output drain capacitance). Input capacitance is measured with all other inputs tied to ground.

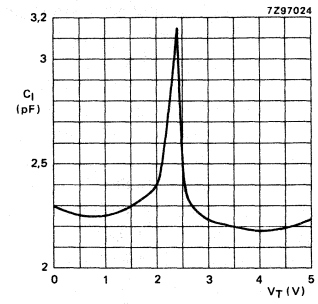


Fig. 26 Typical input capacitance C_I of a 74HC device as a function of input voltage; V_{CC} = 5 V; T_{amb} = 25 °C.

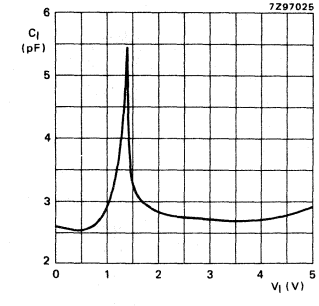


Fig. 27 Typical input capacitance C_I of a 74HCT device as a function of input voltage; V_{CC} = 5 V; T_{amb} = 25 °C.

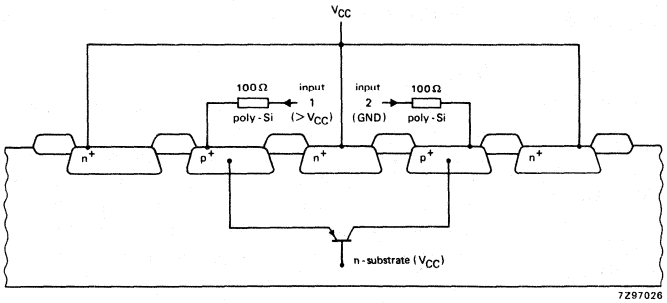


Fig. 28 Cross-section of the input protection of an HCMOS device showing the parasitic pnp transistor between adjacent inputs.

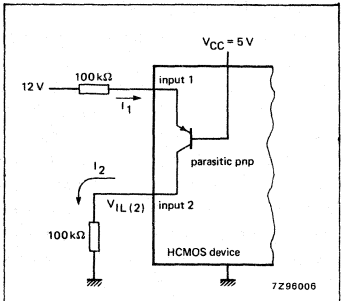


Fig. 29 12 V-to-5 V logic-level conversion at HCMOS inputs using 100 kΩ series resistors.

Coupling of adjacent inputs

Parasitic bipolar pnp transistors can be present between adjacent inputs, e.g. between an input protection diode to V_{CC} and the same diode at the adjacent input, as shown in Fig.28. If the recommended operating input voltage is exceeded, perhaps by ringing of more than 0.7 V, current into the terminal (I_1) can cause a current I_2 in the parasitic transistor and in the adjacent input (Fig.29). Because I_2 in the adjacent input has to be drained by the source driving that input, the source resistance (R) must be low. If R is not low enough, the parasitic current can lift the source voltage and cause unwanted switching.

The ratio of the parasitic adjacent input current (I_2) to the forced input current (I_1) denoted α:

$$\alpha = \frac{I_2}{I_1}.$$

α has been reduced to less than 0.05 (typically 0.001) in the HCMOS family by the use of deep guard rings and optimum bonding pad spacing.

A low α permits proper logic operation in the presence of transients and also allows HIGH-to-LOW voltage translation simply by adding series input resistors. For example, in Fig.29, 12 V system logic is converted to 5 V system logic by adding a 100 kΩ resistor in each input. Since the logic signals are delayed by 1-2 μs, this arrangement is suitable for rather slow 12 V control logic such as that in automotive applications. When the input diodes are used as clamps for logic level translation, the total input current should be limited to 20 mA.

Input voltage and forward diode input current

As a general rule, CMOS logic devices with input clamp diodes (Fig.16) should be operated between the power supply rails. Neglecting the input series polysilicon resistor shown in Fig.16, this means: $-0.5\,V \leqslant V_I \leqslant V_{CC} + 0.5\,V$.

This rule is JEDEC Std. No. 7 and is intended to prevent users damaging devices similar to HCMOS that do not have the polysilicon resistor. HCMOS devices however meet the tougher rating: $-1.5\,V \leqslant V_I \leqslant V_{CC} + 1.5\,V$. Furthermore, virtually all HCMOS devices can operate reliably up to the rating without logic errors.

The maximum permissible continuous current forced into an input or output of a HCMOS device is ±20 mA (JEDEC rating).

OUTPUT CIRCUITS

Output drive

There are three different output configurations in the HCMOS family:

- push-pull
- three-state
- open-drain n-channel transistor.

Each is available with a standard output or a bus driver output, the latter having 50% more drive capability. All 74HC and 74HCT outputs are buffered for consistent current drives and a.c. characteristics throughout the HCMOS family. Well-matched output n-channel and p-channel transistors give symmetrical output rise and fall times.

When comparing the output drive capabilities of HCMOS with those of LSTTL, note that LSTTL capability is usually expressed in unit loads (ULs) where the load is specified to be an input of the same family. This guarantees that a system will operate correctly with worst-case LOW and HIGH input signals and that noise immunity margins will be preserved. HCMOS capability is expressed as the source or sink current at a specified output voltage. Since HCMOS requires virtually no input current, the unit load concept is not applicable.

With a specified output drive of 4 mA (at V_{OLmax} = 0.4 V), the HCMOS capability exceeds 4000 ULs, and with a 20 μA (at V_{OL} = 0.1 V) specification the HCMOS capability is 20 ULs. A standard HCMOS output can drive ten LSTTL loads and maintain $V_{OL} \leqslant 0.4$ V over the full temperature range. A bus driver output can drive 15 LSTTL loads under the same conditions. Table 10 shows the output drive capabilities of some HCMOS devices expressed in LSTTL unit loads. The output current may be increased for higher output voltages. For example, extrapolating the 6 mA bus driver capability at V_{OL} = 0.33 V and T_{amb} = 85 °C to a V_{OL} of 0.5 V gives an output drive capability of 9 mA.

Output current derating as a function of temperature is shown in Fig.30 and is valid for all types of output. Output source and sink drives at V_{CC} = 2 V, 4.5 V and 6 V are given in Figs.31 to 34 which show the output current as a function of output voltage; these graphs indicate the typical output currents and the expected minimum output currents. They can serve as a design aid when calculating transmission line effects or when charging highly capacitive loads.

The expected minimum curves are not guaranteed; they are tested only at the values given in the data sheets.

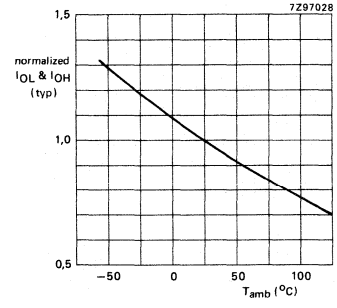
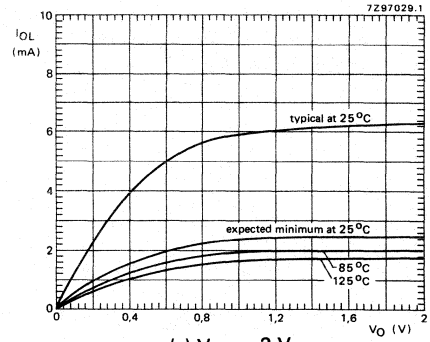


Fig. 30 Derating curve for output drive currents I_{OL} and I_{OH}.

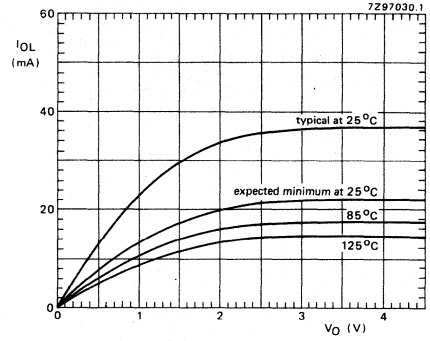
Table 10: Comparison of the output drive capabilities of LSTTL and HCMOS ($V_{OL} \leqslant 0.4$ V)

LS device	output	drive capacity	HCMOS equiv.	type	output	drive capacity
74LS00	4 mA	10 UL	74HC00	standard	4 mA	10 UL
74LS138	4 mA	10 UL	75HC138	standard	4 mA	10 UL
74LS245	12 mA	30 UL	74HC245	bus	6 mA	15 UL
74LS374	12 mA	30 UL	74HC374	bus	6 mA	15 UL

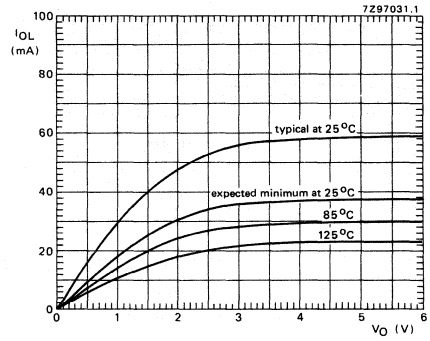
UL = unit load.



(a) V_{CC} = 2 V

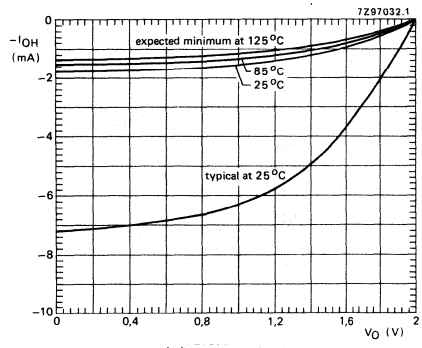


(b) V_{CC} = 4.5 V

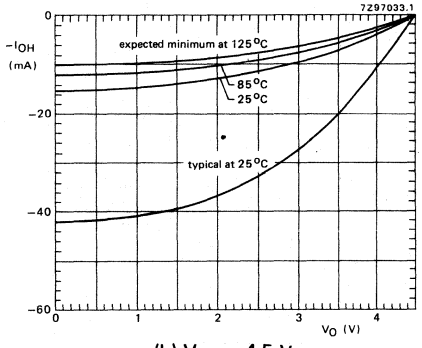


(c) V_{CC} = 6 V

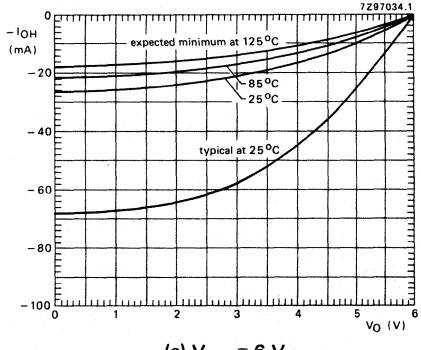
Fig. 31 Standard output n-channel sink current.



(a) V_{CC} = 2 V

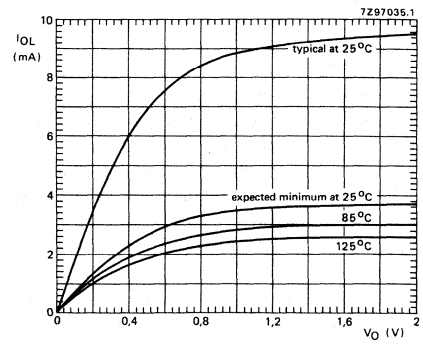


(b) V_{CC} = 4.5 V

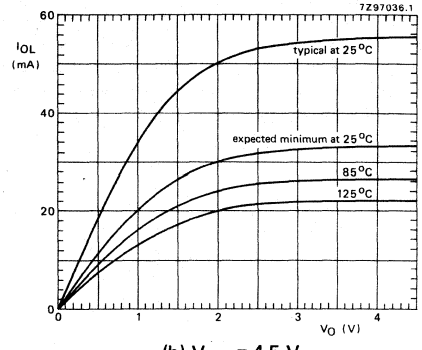


(c) V_{CC} = 6 V

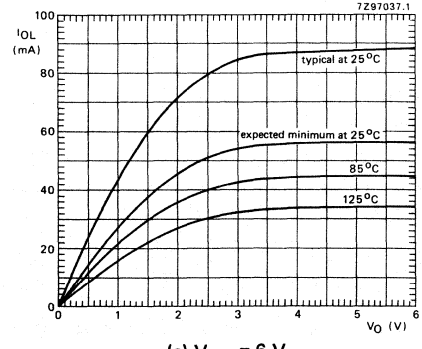
Fig. 32 Standard output p-channel source current.



(a) V_{CC} = 2 V

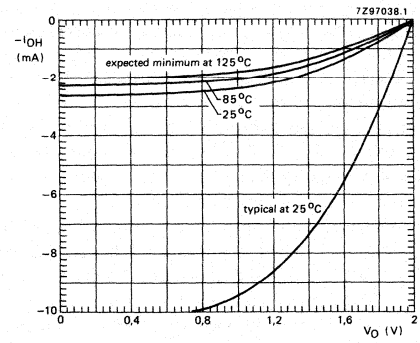


(b) V_{CC} = 4.5 V

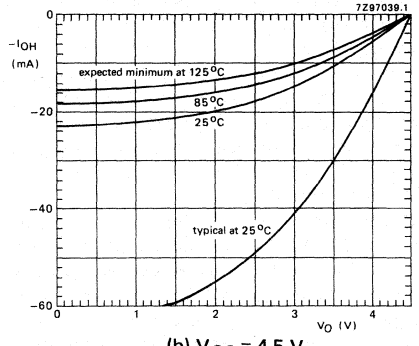


(c) V_{CC} = 6 V

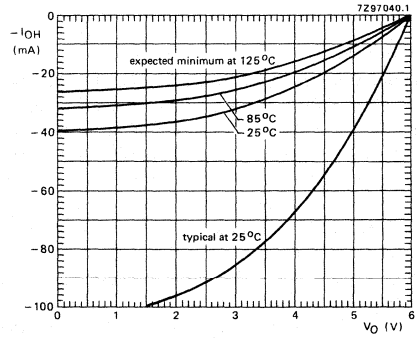
Fig. 33 Bus-driver output n-channel sink current.



(a) V_{CC} = 2 V



(b) V_{CC} = 4.5 V



(c) V_{CC} = 6 V

Fig. 34 Bus-driver output p-channel source current.

Push-pull outputs

A typical push-pull output stage is shown in Fig.35. The bipolar parasitic transistor-drain diodes (D1 and D2) limit the output voltage V_O of all HCMOS devices in the case of externally-forced voltages such that $-0.5\ V \leqslant V_O \leqslant V_{CC} + 0.5\ V$. For voltages outside this range, the diodes and parasitic bipolar elements start to conduct. Although the diode current rating is 20 mA d.c., line ringing and power supply spikes in normal high-speed systems cause current-peaks that exceed this rating. Careful chip-layout and adequate aluminium traces ensure that the current peaks produced will not damage the diodes or degrade the internal circuitry.

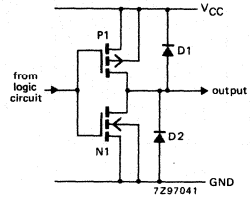


Fig. 35 Basic CMOS output stage.

The maximum rated d.c. current for a standard output is 25 mA and that for a bus-driver output is 35 mA. These ratings are dictated by the current capability of on-chip metal traces and long-term aluminium migration, but it is expected that output currents during switching transients will, at times, exceed the maximum ratings.

A shorted output will also cause the maximum d.c. current rating to be exceeded. However, for logic testing, one output may be shorted for up to five seconds without damaging the device.

Three-state outputs

In the typical three-state output circuit shown in Fig.36, when EO is HIGH the output is enabled and transistors P4 and N4 act as a transmission gate connecting the gates of the output transistors. A LOW at EO puts the output in the high-impedance OFF-state and transistors P3 and N3 act as pull-up and pull-down transistors respectively. The logic symbol for a three-state output and its function table is shown in Fig.37.

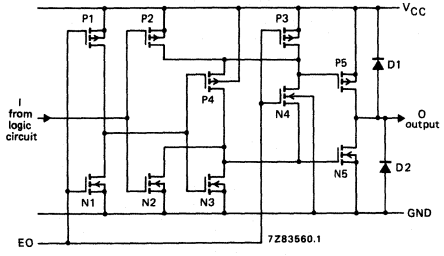
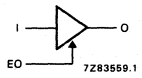


Fig. 36 Typical three-state output circuit.



(a) logic symbol

inputs		outputs
I	EO	O
X	L	Z
L	H	L
H	H	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

(b) function table

Fig. 37 Three-state output logic symbol and functions.

Three-state outputs are designed to be tied together but are not intended to be active simultaneously. To minimize noise and to protect outputs from excessive power dissipation, only one three-state output should be active at any time. In general, this requires that the output enable signals should not overlap. When decoders are used to enable three-state outputs, the decoder should be disabled while the address is being changed. This avoids overlapping output-enable signals caused by decoding spikes to which all decoder outputs are prone during address-changing.

When designing with three-state outputs, note that disable propagation delays are measured for an RC load when the output voltage has changed by 10% of the voltage swing. This 10% level is adequate to ensure that a device output has turned off. Although this method provides a standard reference for measuring disable times, it implies that the output is already off for 10% of the RC time. Because all disable times are measured with a load of 1 kΩ and 50 pF, subtract the 10% RC time (5 ns) from the values published in the data sheets to obtain the real internal disable propagation delay.

Diodes D1 and D2 are parasitic diodes associated with output transistors P5 and N5 respectively. Diode D1 clamps the output at one V_{BE} above V_{CC}, of importance in large systems where sections of the system may be powered-down (V_{CC} = 0 V), in which case the output diode current has to be limited to 20 mA.

All I/O ports and transceivers have a three-state output as shown in Fig.36. The I/O pin is defined as an input when the output is disabled, but this pin should be regarded as a real input and should not be left floating, because the input to an I/O port can cause V_{CC} current. If necessary, terminate the input with a 10 kΩ resistor, see 'Termination of unused inputs'.

Open-drain outputs

In TTL families, several functions are offered with open-collector outputs to enhance logic functions by using OR-tied logic. The advantage of OR-tied logic is the logic elements saved and hence the lower power dissipation. However, this is countered by power loss and reliance on RC time propagation delays. These disadvantages are not encountered in CMOS and similar applications can be made using devices with 3-state outputs, or simply with the power-saving logic devices. However, the 74HC/HCT03 (quad 2-input NAND gate) has an open-drain n-channel output, see Fig.38. The parasitic diode D1 is not present (there being no p-channel transistor); this allows the output voltage to be pulled above V_{CC} to V_{Omax} making both HIGH-to-LOW and LOW-to-HIGH level-shifting possible. For digital operation, a pull-up resistor is necessary to establish a logic HIGH level.

The open-drain output is protected against electrostatic discharge.

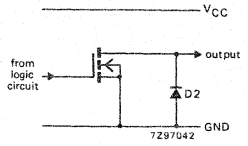


Fig. 38 Open-drain output circuit.

Increased drive capability of gates

To increase output drive, the inputs and outputs of gates in the same package may be connected in parallel. It is advisable to restrict parallel connection to gates within one package to avoid large transient supply currents due to different gate-switching times.

For further information, see chapter 'Interfacing and protection of circuit board inputs'.

Output capacitance

For push-pull outputs, no output capacitance is specified because either the n-channel transistor or the p-channel transistor creates a low-impedance path to the supply rails.

Three-state outputs can be switched to the high impedance OFF-state, and because many of them can be connected to a bus line, the output capacitance is needed to calculate the total capacitive load. For bus-driven 3-state outputs in a DIL package, the output capacitance is 6 pF (typ.) and 20 pF (max.).

STATIC NOISE IMMUNITY

The static noise immunity can be divided into:

- the static noise margin LOW. This is the voltage difference between V_{ILmax} of the driven device and V_{OLmax} of the driver.
- the static noise margin HIGH. This is the difference between V_{OHmin} of the driver and V_{IHmin} of the driven device.

For 74HC devices, both the LOW level noise margin and the HIGH-level noise margin is 28% of V_{CC}. This is a considerable improvement over LSTTL where the LOW-level noise margin is only 8% of V_{CC} and the HIGH level noise margin is just 14% of V_{CC}. The margins are even greater for HCMOS at higher supply voltages as shown in Fig.39. As 74HCT devices have the same switching levels as LSTTL, their noise margins are also the same.

The superior noise immunity of the 74HC input can be clearly seen from the voltage levels of the input-to-output transfer characteristics shown in Figs.40 and 41.

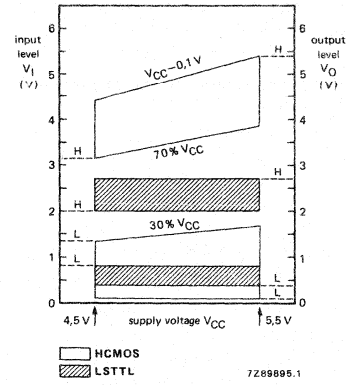


Fig. 39 Worst-case input and output voltages over an operating supply range of 4.5 V to 5.5 V.

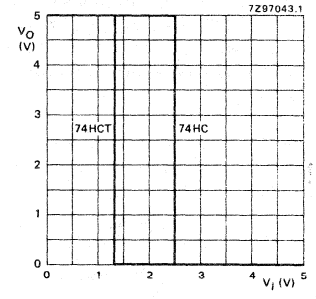


Fig. 40 Typical input-to-output transfer characteristic for 74HC and 74HCT devices.

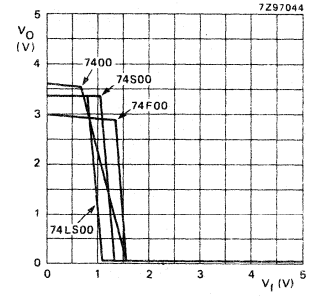


Fig. 41 Input-to-output transfer characteristics for TTL devices.

Table 11 shows the input noise margin of HCMOS devices where like devices are interfaced. Output voltages are also given.

Table 11: Noise immunity and noise margin for HCMOS devices (V_{CC} = 4.5 V)

		74HC	74HCT	74HCU
V_{ILmax}	(V)	1.35	0.8	0.9
V_{IHmin}	(V)	3.15	2	3.6
V_{OLmax}	(V)	0.1	0.1	0.5
V_{OHmin}	(V)	4.4	4.4	4
Noise margin low				
V_{NML}	(V)	1.25	0.7	0.4
Noise margin high				
V_{NMH}	(V)	1.25	2.4	0.4

Table 12 shows the input noise margin of 74HCT devices interfacing with LSTTL devices; the 74HCT or LSTTL output is fully-loaded, V_{CC} = 4.5 V and T_{amb} is 0 °C to +70 °C (the only convenient temperature range when using LSTTL characteristics).

Table 12: Noise immunity and noise margin for 74HCT and LSTTL device interfacing

		74HCT	LSTTL
V_{ILmax}	(V)	0.8	0.8
V_{IHmin}	(V)	2	2
V_{OLmax}	(V)	0.33 (note 1) 0.1 (note 2)	0.4
V_{OHmin}	(V)	3.84 (note 1) 4.4 (note 2)	2.7
Noise margins (V):			
from 74HCT to LS		V_{NML}	0.47
		V_{NMH}	1.84
from LS to 74HCT		V_{NML}	0.4
		V_{NMH}	0.7
from LS to LS		V_{NML}	0.4
		V_{NMH}	0.7
from 74HCT to 74HCT		V_{NML}	0.7
		V_{NMH}	2.4

Notes

1. 4 mA load (i.e. 10 LSTTL inputs).
2. 20 μA load (i.e. 20 74HCT inputs).

Whenever a 74HCT output drives either an LSTTL or a 74HCT input, the noise margin is better than when an LSTTL device drives an LSTTL or 74HCT input. This improvement is larger for V_{NMH} owing to the superior output sourcing current of the rail-to-rail HCMOS output swing compared with the limited totem-pole pull-up output voltage of LSTTL.

DYNAMIC NOISE IMMUNITY

As for static noise immunity, dynamic noise immunity can be divided into two parts:

- a dynamic noise margin LOW
- a dynamic noise margin HIGH.

For 74HC devices, both margins are similar; for 74HCT devices, the dynamic noise margin LOW is the smaller of the two. To plot it, a pulse of known magnitude, V_p, is applied to the input of a device and its width, t_W, is increased until the device just begins to switch. The input level on which V_p is based is equal to the switching voltage minus the worst-case static noise margin LOW. The pulse width is measured at half pulse height, $V_p/2$. The rise and fall times, t_r and t_f are 0.6 ns.

V_p is then reduced in increments and t_W for each new value is ascertained.

The test is repeated for different supply voltages — for 74HC devices between 2 V and 6 V, and at 5 V for 74HCT devices. A range of output currents, I_O, are also used. Increasing the d.c. load reduces the dynamic noise immunity.

Figure 42 shows the amplitude of positive-going pulses that can be withstood in the LOW state for 74HC and 74HCT devices. The curves are worst-case ones with fully-loaded drivers, so a system using only 74HC or 74HCT devices will have 0.23 V more noise margin for all t_W.

For typical input switching thresholds of 1.4 V and 2.25 V for 74HCT (V_{CC} = 5 V) and 74HC (V_{CC} = 4.5 V) respectively, the noise margins will be 0.83 V [(1.4 − 0.8) + 0.23 V] larger for 74HCT and 1.13 V [(2.25 − 1.35) + 0.23 V] larger for 74HC devices.

The main causes of unwanted input pulses are spikes due to outputs switching, which dumps large currents on the GND lines, or reflections when long lines (longer than about 32 cm) are driven. For more information on the latter, see chapter 'Replacing LSTTL and driving transmission lines'.

The best example of an unwanted pulse generator is an octal device with bus outputs of which seven are switching simultaneously and the eighth, most remote, output is LOW. Figure 43(a) shows the maximum pulse voltage measured on the unswitched output of a 74HC/HCT374 as a function of V_{CC}. Figures 43(b) and 43(c) show this maximum volt-

age and the pulse width as functions of the number of outputs that are switching. It should be emphasised that any pulses produced by switching outputs won't cause other devices to respond even in worst-case conditions. This is because Fig.42 is based on a worst-case V_{OL} and the maximum expected pulse height of Fig.43 occurs for a best-case V_{OL}. So, even when a pulse of the maximum expected height shown in Fig.43 occurs, there is still a noise margin. This can be verified by plotting the pulse heights of Fig.43 on the curves of Figs.42(a) and 42(b).

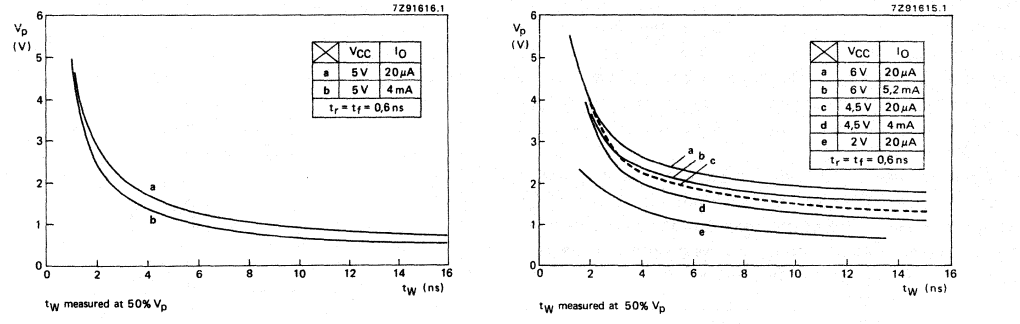


Fig. 42 Amplitude of the positive-going pulses that can be withstood in the LOW state (worst-case, fully-loaded driver) for (a) 74HC devices and (b) 74HCT devices.

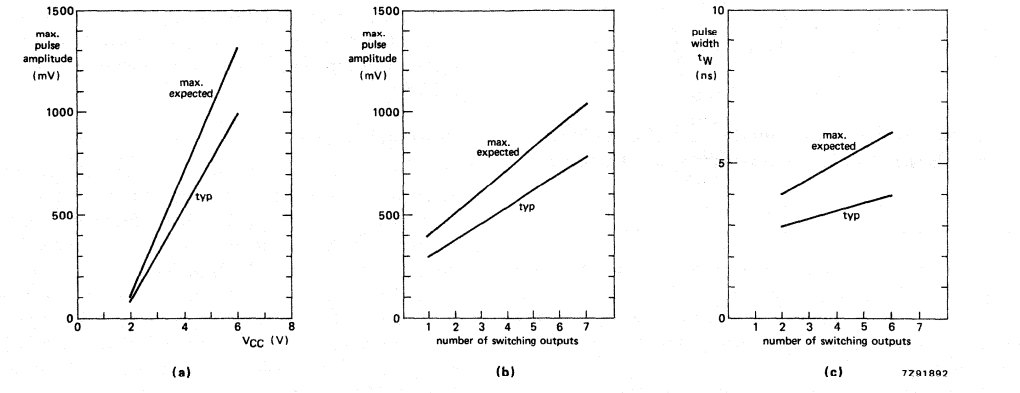


Fig. 43 (a) Amplitude of the voltage pulse (on pin 2, the most remote) due to switching seven of the bus-driver outputs of a 74HC/HCT374 octal flip-flop; C_L = 150 pF, T_{amb} = 25 °C. (b) Amplitude of the voltage pulse (on pin 2) as a function of the number of outputs switched; V_{CC} = 5 V, C_L = 150 pF. (c) Pulse width as a function of the number of outputs switched; V_{CC} = 4.5 to 6 V, C_L = 150 pF. For V_{CC} = 2 V, the maximum expected pulse width is about 10 ns.

BUFFERED DEVICES

Definition

Often the terms 'buffer devices', 'buffered inputs' or 'buffered outputs' are used without qualification and originate from the very first unbuffered CMOS logic family consisting of one-stage logic elements, usually gates. In these devices, both input switching levels and output impedances were not constant, so neither were output rise/fall times or propagation delay times. The Jedec JC40.2 committee define a buffered device to be at least two active stages with the output independent of the input logic voltage level and independent of the number of inputs that are HIGH or LOW.

A buffer meeting this definition is the AND-function circuit of Fig.44. The gain between input and output is high enough to consider the output impedance to be independent of the logic level at the input, and the output impedance is not affected by the state of the logic inputs.

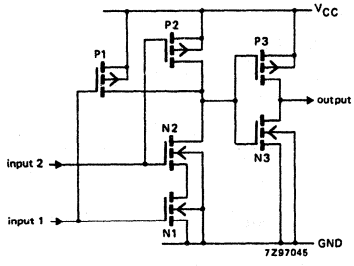


Fig. 44 The minimum number of stages for a buffered device is two. This 2-stage example is an AND function.

All 74HC and 74HCT devices comprise at least two stages to minimize any pattern sensitivity of propagation delay time. Buffering also improves static noise immunity due to increased voltage gain, giving almost ideal transfer characteristics.

The designation 74HCU is used to denote single-stage devices. These have the same specification as 74HC devices but their input and output voltage parameters are relaxed. 74HCU devices don't have the high gain of 74HC/HCT versions, which makes them more suitable for use in RC or crystal oscillators and other feedback circuits operating in the linear mode.

Output buffering

All 74HC and 74HCT devices have buffered outputs for optimum performance. To demonstrate the benefits of output buffering, consider what would happen without it. In the single-stage device shown in Fig.45, the output impedance depends on the d.c. input voltage. Consequently, the noise margins at the output become a function of the input voltage, even when V_I is a legal HIGH or LOW level.

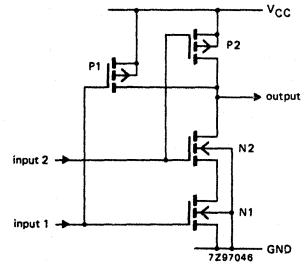


Fig. 45 Unbuffered NAND gate.

The steady-state impedance of the circuit of Fig.45 is also affected by the state of the inputs. Given that P1 and P2 have identical performances (same size), there are two values of impedance for output HIGH; one when either input is LOW and P1 or P2 conducts, and another when both inputs are LOW and both P1 and P2 conduct. Therefore, without output buffering, the state of output conduction depends on the number of inputs that are HIGH or LOW.

Input buffering

An input is considered to be buffered when its switching threshold is unaffected by the logic states of other inputs. In the example of Fig.45 that has unbuffered inputs, the switching threshold of input 1 varies with a HIGH level at input 2, and vice versa. This is because the series impedance of transistors N1 and N2 determines the switching threshold of the device. The result can be seen in Fig.46 where curve 1+2 occurs when the two inputs are tied together, and curve 1 or 2 is the switching threshold when the accompanying input is at V_{CC}.

For true input buffering, an input must have an inverter stage with sufficient gain to ensure that logic levels give independent on-chip levels. Some gates in the 74HC series (usually AND or OR gates) have unbuffered inputs, however all devices meet the family logic level requirements. All 74HCT devices have buffered inputs.

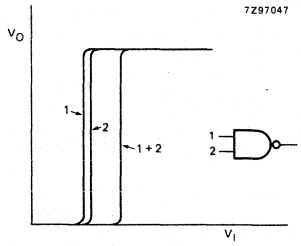


Fig. 46 Example of different switching levels in unbuffered inputs.

PERFORMANCE OF OSCILLATORS

When HCMOS devices are used in RC, crystal or Schmitt trigger oscillators or in analog amplifiers:

- a supply voltage of at least 3 V is required. Below this value, the transconductance of crystal oscillators is too low to start oscillations. In analog circuits, insufficient output current is available to drive external components;
- slow input rise and fall times cause the input stage of a HCMOS device to draw current. This additional quiescent supply current ΔI_{CC} is given in the data sheets for 74HCT devices since these can be used as LSTTL replacements and may be driving a significant load. The total I_{CC} for 74HC devices can be calculated by multiplying the value of I_{CC} read from Fig.12 by the unit load coefficient given in the data sheet for the 74HCT device;
- in general, frequency stability won't be affected by supply voltage, so long as the permissible output currents of the devices are not exceeded.

For further information, see chapters 'Crystal oscillators' and 'Astable multivibrators'.

LATCH-UP FREE

Latch-up is the creation of a low-impedance path between the power supply rails caused by the triggering of parasitic bipolar structures (SCRs) by input, output or supply overvoltages. These overvoltages induce currents that can exceed maximum device ratings. When the low-impedance path remains after removal of the triggering voltage, the device is said to have latch-up.

The JEDEC standard test being developed for latch-up specifies that the input/output current should be equal to the maximum rating (±20 mA), and that V_{CC} should also be not more than twice V_{CCmax} (14 V) for testing latch-up immunity with excess supply voltage. HCMOS ICs have been extensively subjected to the previously described tests with test parameters far exceeding those quoted by JEDEC. In no case did latch-up occur. For example, it has been determined that an HCMOS input can typically withstand continuous current (5 s on, 15 s off) of 100 mA to 120 mA, or 1 μs pulses of 300 mA with a duty factor of 0.001. An input can also withstand a discharge from a 200 pF capacitor charged to 330 V. An HCMOS output can withstand continuous current (5 s on, 15 s off) of 200 mA to 300 mA, or 1 μs pulses of 400 mA with a duty factor of 0.001. However, because there is an internal polysilicon 100 Ω resistor in series with all HCMOS inputs, the input voltages required to achieve these current levels are so high ($V_I = V_{CC} + 0.7\,V + 100I_I$) that it is unlikely that they could occur in practice, even in a 6 V system with severe glitches. Moreover, beyond these current levels, excessive heating occurs or aluminium tracks or bond wires breakdown. It is therefore reasonable to conclude that HCMOS logic ICs are completely latch-up free.

For further information, see chapter 'Standardizing latch-up immunity tests'.

DROP-IN REPLACEMENTS FOR LSTTL

74HCT devices are power-saving, drop-in replacements for LSTTL devices. Because most systems are operated at frequencies far below the maximum possible, 74HCT devices can also be used to good effect in systems using ALS, AS, S, and FAST devices.

Fan-out should be considered when replacing a TTL device by a 74HCT device. TTL fan-out is usually expressed in unit loads (ULs) and the load is specified to be an input of the same family. In fact, TTL fan-out is determined by the ability of the outputs to sink current (a TTL input usually sources current). Table 13 shows the fan-out of 74HCT to the different TTL families.

The fan-outs given in Table 13 are derived at a voltage drop of max. 0.4 V (V_{OL}). In the "74" TTL series, an extended V_{OL} figure is often seen, e.g. 8 mA at 0.5 V voltage drop for LSTTL. If this figure is used to determine the fan-out of the TTL device it can result in a higher fan-out than is possible with 74HCT. This can be resolved by replacing as many of the driven TTL parts as possible by 74HCT devices to reduce the sink current requirement (the 74HCT input current is negligible). In addition, power dissipation is reduced significantly by using 74HCT.

Table 13: Fan-out of 74HCT to TTL circuits

74HCT	TTL	LS	ALS	FAST	S & AS
standard output	2	10	20	6	2
bus-driver output	3	15	30	10	3

BUS SYSTEMS

CMOS is being used to an increasing extent in microprocessor bus systems following the introduction of versions of the popular NMOS processors.

There are several constraints imposed on microprocessor systems in industrial applications, such as electrically-noisy environments, battery-standby requirements and sealed, gas-tight enclosures. HCMOS bus systems, e.g. the CMOS STD bus (a non-proprietary CMOS bus standard) provides a solution to all these problems. It offers superior noise immunity, equal operating speed, lower power dissipation, wider supply voltage range, extended temperature range, and enhanced reliability.

For optimum results, use only 74HC devices in circuits which communicate directly with the bus. This allows a new bus termination to be introduced (see Fig.47(b)) which, unlike the conventional TTL bus termination, draws no heavy d.c. current and is more suited to HCMOS outputs.

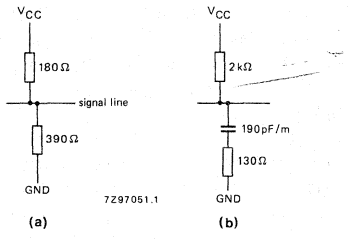


Fig. 47 Bus terminations. (a) Conventional termination for TTL buses. (b) Proposed termination for CMOS STD bus equivalents.

The wider supply voltage range of HCMOS together with its lower power dissipation virtually eliminates problems caused by voltage drops along power buses between cards in a system. It is possible for a circuit to pick up severe noise spikes or differential voltages via an edge connector. Such pick-up can exceed the CMOS maximum ratings if not limited by a 10 kΩ series resistor in the HCMOS logic line. This will limit current to ±20 mA for external voltages of up to ±200 V, however, for correct functioning, the d.c. input current should be kept below those values stated in 'Input/output protection'. The recommended board edge input protection is shown in Fig.48.

In the circuit of Fig.48, if the input diode current exceeds the maximum input current, a HIGH-to-LOW level shifter should be used (e.g. 74HC4049 or 74HC4050).

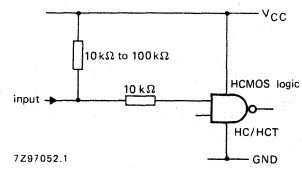


Fig. 48 Example of the board edge input protection circuit.

For further information, see chapter 'Interfacing and protection of circuit board inputs'.

Since HCMOS bus-drivers do not have built-in hysteresis, slowly-rising pulses should be avoided or devices with Schmitt-trigger action should be used, such as the flip-flop series 74HC/HCT73, 74, 107, 109, 112, or the dedicated Schmitt triggers 74HC/HCT14 and 132. The rise and fall times can be derived from the information given in the section 'Propagation delays and transition times' of this User Guide.

PACKAGE PIN CAPACITANCE

In purely digital circuits, the input capacitance or three-state output capacitance is sufficient to determine the dynamic characteristics. However, when a HCMOS device is used in the linear region, it is necessary to take pin capacitance into account, e.g. to prevent crosstalk in analog switches or peaks in the frequency response of PLLs.

The use of SO packages with their low pin capacitances is recommended for HCMOS analog designs. Table 14 gives the pin-to-pin capacitances for the plastic DIL and SO packages used for HCMOS. Measurements were made using a dummy package with all unused pins connected to ground.

Table 14: Typical pin capacitances (pF) of SO and DIL packages

	SO-14 & SO-16	DIL-16	SO-20	DIL-20	SO-24	DIL-24
capacitance to ground of:						
corner pins	0.41	0.97				
all other pins	0.21	0.37				
any end two pins			0.65	1.12		
all other pins			0.25	0.40		
any end three pins					0.65	1.64
all other pins					0.33	0.65
capacitance between adjacent pins:						
including a corner pin	0.15	0.40				
all other pins	0.04	0.13				
any end three pins			0.28	0.49		
all other pins			0.14	0.22		
any end three pins					0.30	0.70
all other pins					0.12	0.28

APPLICATION NOTES

INTERFACING AND THE PROTECTION OF CIRCUIT BOARD INPUTS

Because the operating speed of 74HC/HCT/HCU high-speed CMOS (HCMOS) logic ICs is comparable to that of LSTTL but their power dissipation is much less, the interfaces between these two logic families are of the most general interest. We have therefore dealt extensively with this subject in a separate article entitled "Replacing LSTTL and driving transmission lines". Interfacing HCMOS with LSTTL ICs will not therefore be discussed again here. This article describes interfacing HCMOS ICs with commonly used logic families other than LSTTL, namely, HE4000B series CMOS and the ECL 10K family. It also discusses interfacing HCMOS with non-standard levels (12 V to 24 V) and driving external loads which are often encountered in industrial control and automotive applications. Methods of protecting HCMOS inputs at pcb interfaces are also described. Table 1 gives an overview of the requirements for interfacing HCMOS ICs with all commonly used IC logic families (including TTL).

INTERFACING HCMOS WITH HE4000B SERIES CMOS

HCMOS ICs can be coupled directly to standard HE4000B series CMOS ICs if both families operate from the same supply voltage. However, if the IC families have different supply voltages, level shifting is necessary. The configuration shown in Fig.1(a) illustrates this for an HCMOS IC driving an HE4000B IC via an HEF4104B level-shifter. Note that the HEF4104B is exclusively a LOW-to-HIGH level-shifter and care should be taken to ensure that V_{CC1} never exceeds V_{CC2} by more than one V_{BE}.

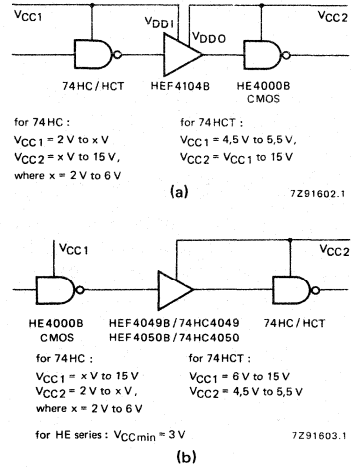


Fig.1 Interfacing HCMOS with HE4000B logic; (a) an HCMOS IC driving an HE4000B series CMOS IC; (b) an HE4000B series CMOS IC driving an HCMOS IC

TABLE 1
Interfacing HCMOS to other logic families

		TO					
		74HC 5 V supply	**74HCT** 5 V supply	**HE4000B** 5 V supply	**HE4000B** 6–15 V supply	**TTL*** 5 V supply	**ECL 10K**
FROM	**74HC** 5 V supply	direct	direct	direct	4104	direct	10124
	74HCT 5 V supply	direct	direct	direct	4104	direct	10124
	HE4000B 5 V supply	direct	direct	direct	4104	direct	10124
	HE4000B 6–15 V supply	4049 or 4050	4049 or 4050	4049 or 4050	direct	4049 or 4050	transistor
	TTL* 5 V supply	pull-up resistor	direct	pull-up resistor	4104	direct	10124
	ECL 10K	10125	10125	10125	transistor	10124	direct

* Includes LS, S, STD, FAST, ALS and AS.

Figure 1(b) shows how to drive an HCMOS IC from an HE4000B IC using an HEF4049B/4050B or 74HC4049/4050 HIGH-to-LOW level shifter. Since these level shifters don't have an input clamping diode to V_{CC}, the maximum input level is 15 V. The logic level switching threshold remains referenced to V_{CC2}, so the LOW noise margin will be the same as that for the 5 V specification.

For interfacing HCMOS ICs with NMOS microprocessors, memories, etc., the rules for TTL apply because NMOS ICs usually have TTL-compatible inputs and outputs. The only exceptions are NMOS ICs with open-drain outputs where a pull-up resistor must be used to load the output.

INTERFACING HCMOS WITH ECL 10K LOGIC

To drive HCMOS from ECL 10K logic, the ECL 10125 ECL-to-TTL translator is used as shown in Fig.2(a). To drive ECL 10K logic from HCMOS, the ECL 10124 TTL-to-ECL translator is used as shown in Fig.2(b). Note that, since these translators operate at TTL levels, pull-up resistor R_1 is necessary if the ECL 10125 is used to drive a 74HC IC as shown in Fig.2(a). This technique is not favoured because the time-constant formed by the pull-up resistor and the combined stray and load capacitance increases the propagation delay and also make it less predictable. Although reducing the value of R_1 minimizes the increase of propagation delay, the resistor then dissipates more power and reduces the LOW noise margin. Using R_1 also increases production costs because it requires board space and has to be inserted. All of these drawbacks conflict with the purpose of using HCMOS to increase system performance and reduce power dissipation. The pull-up resistor should therefore only be used if it is absolutely unavoidable. A better solution is to use a 74HCT IC as the driven element because the 74HCT range of ICs have TTL-compatible inputs.

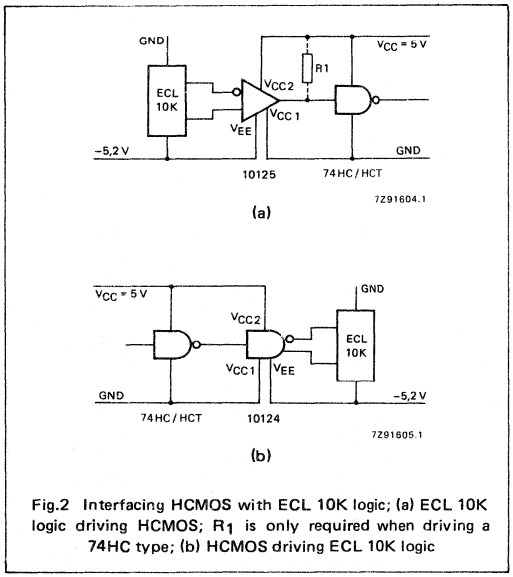


Fig.2 Interfacing HCMOS with ECL 10K logic; (a) ECL 10K logic driving HCMOS; R_1 is only required when driving a 74HC type; (b) HCMOS driving ECL 10K logic

INTERFACING HCMOS WITH NON-STANDARD LOGIC LEVELS

In many applications, there is a need to interface HCMOS ICs with non-standard input and output levels. For example, in industrial control or automotive systems powered by a 12 to 24 V supply. The circuits in Figs.3(a) and 3(b) show the basic configurations for these interfaces.

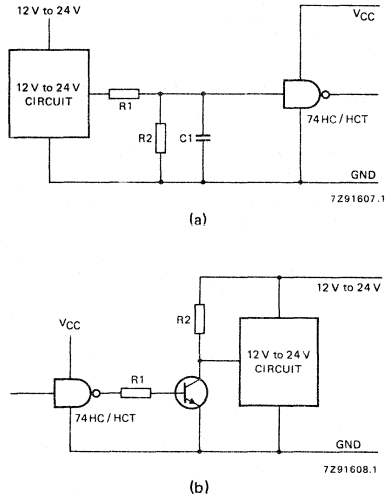


Fig.3 Interfacing HCMOS with non-standard logic levels; (a) driving HCMOS with non-standard logic levels. The values of R_1 and R_2 depend on the output voltage of the driving circuit and the value of C_1 depends on the noise and speed; (b) HCMOS driving a system with non-standard logic levels. The values of R_1 and R_2 depend on the supply voltage and the type of transistor

HCMOS DRIVING EXTERNAL LOADS

The configuration for HCMOS ICs driving loads connected to a supply voltage greater than V_{CC} is given in Fig.4(a). Figure 4(b) and 4(c) show methods of using an HCMOS IC to drive a load (for example, a relay) connected to the same supply as the IC.

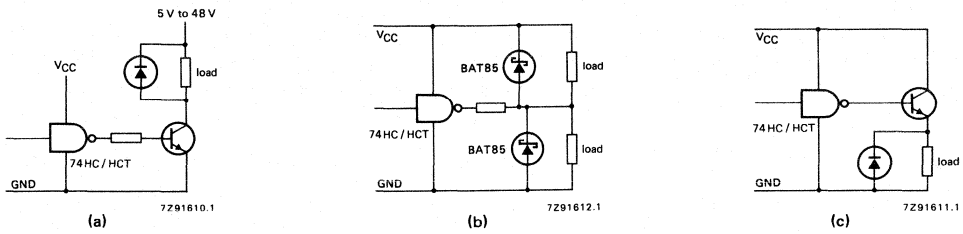


Fig.4 HCMOS driving external loads: (a) HCMOS needs a transistor interface to drive a load connected to an external supply greater than V_{CC}; (b) HCMOS driving a split load connected to V_{CC}; (c) HCMOS driving a single load connected to V_{CC}

PROTECTING HCMOS INPUTS CONNECTED DIRECTLY TO A BOARD INTERFACE

All HCMOS ICs have input protection circuitry that can withstand normally anticipated electrostatic discharge (ESD). However, an input that is connected directly to a signal source outside the pcb can be exposed to potentially damaging voltage levels during:

- transport
- servicing (connection to high external voltage)
- partial system power-down
- operation when parts of the system are faulty.

For this reason, additional protection is required for inputs that receive signals from outside the pcb. A simple input protection circuit is shown in Fig.5. It consists of:

- a pull-up resistor to ensure that the input is in a defined logic state, even when the drive is disconnected
- a series resistor which, in the event of high level input voltages, limits the input protection diode current to a safe level.

The value for the pull-up resistor is easy to determine because it only passes the input leakage current, and therefore causes very little voltage drop, when the board supplying the drive is disconnected. A value of 100 kΩ gives a good compromise between power consumption and noise sensitivity.

The value of the series resistor depends on the parasitic input capacitance and wiring capacitance. Any external resistance in series with an input will cause additional propagation delay due to increased RC time-constant. The additional propagation delays as functions of the RC time-constant are:

For 74HCT ICs: $t_{PHL} = 1{,}27RC$
$t_{PLH} = 0{,}33RC$

For 74HC ICs: $t_{PHL} = 0{,}7RC$
$t_{PLH} = 0{,}7RC$.

If it is assumed that the parasitic capacitance at each of the two IC inputs in Fig.5 is 3,5 pF, the total input wiring capacitance is 10 pF and the maximum permitted additional propagation delay is 10 ns, then the maximum value for the series resistor is:

$R_{max} = 10\,ns/(1{,}27 \times 17\,pF) = 460\,\Omega$ for a 74HCT IC

$R_{max} = 10\,ns/(0{,}7 \times 17\,pF) = 840\,\Omega$ for a 74HC IC.

From this example, it is clear that a higher value series resistor can be used without significantly increasing the propagation delay if care is taken to minimize the input wiring capacitance. The capacitance can be minimized by observing the following:

- the input capacitance of the ICs cannot be reduced but it may be possible to reduce the number of inputs separately connected directly to a pcb interface
- connect the series resistor as close as possible to the IC input pin
- position the IC and the series resistor as close as possible to the pcb interface.

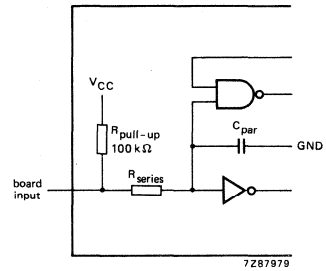


Fig.5 Additional input protection for HCMOS ICs receiving board inputs

STANDARDIZING LATCH-UP IMMUNITY TESTS FOR HIGH-SPEED CMOS LOGIC ICs

Like all other integrated CMOS logic circuits, the 74HC/HCT/HCU family of HCMOS logic ICs contain a number of parasitic 4-layer bipolar structures (SCRs) which may be triggered by current transients caused by high-level voltage transients at the input, output or supply pins. Once one or more of these parasitic structures has been triggered, a low-impedance path exists between the internal supply rails. This pulls the supply voltage down to a low level causing a flow of supply current (several hundred mA) which exceeds $I_{CC\,max}$ and causes excessive or destructive power dissipation. If the low-impedance path between the supply rails persists after the transient has passed (quiescent I_{CC} exceeds the maximum specified value), the IC is said to be in latch-up.

This article discusses the parasitic bipolar structures within HCMOS ICs, and describes the precautions that have been taken during the manufacturing process to minimize their effect. It also describes four test methods which effectively evaluate the input/output currents and the supply overvoltage which are necessary to induce latch-up.

The four tests are:

1. Continuous current (2 ms to 5s) into inputs/outputs with the supply voltage applied either before or after the input/output current has been established. The 5s current duration can only be used if the power dissipation is below 500 mW. This test can be performed with automatic test equipment.
2. Pulsed currents into inputs/outputs (<2 ms). A less worst-case type of test (less heat generation and delay storage effect allows higher currents before latch-up occurs) that creates a more realistic simulation of transients and also allows the test to be automated.
3. Capacitor discharge into inputs to simulate electrostatic discharge.
4. Supply overvoltage.

Extensive application of these tests to several different brands of high-speed CMOS ICs has shown that tests 1 and 4 alone are sufficient to evaluate the sensitivity of any IC to all four types of latch-up stimulus. Since test 2 allows higher test currents to be applied before latch-up occurs, especially when the pulses are very brief (<1 μs) test 1 will indicate the worst-case (lowest) currents required to initiate latch-up.

All latch-up tests published so far lack essential information and require a dedicated test set-up. We therefore propose tests 1 and 4 for use as a standard for evaluating latch-up immunity of high-speed CMOS ICs.

It is also possible to use a transistor curve tracer (Tektronix 576 or similar) to perform tests 1 and 4 to very quickly evaluate the latch-up immunity of HCMOS ICs. The tests performed with a transistor curve tracer have the added advantage of being non-destructive and clearly indicating the V/I relationship after latch-up to indicate the severity of the phenomenon. They also show the 'snap back' voltage (sustaining voltage) after V_{CC} breakdown and the minimum holding current. This gives a good indication of the maximum supply voltage that can be used without parasitic SCRs being triggered. Because bipolar transistor current gain (h_{FE}) and the value of resistors increase with increasing temperature, high ambient temperature or localized die heating results in reduced latch-up immunity.

The JEDEC standard test being developed for latch-up specifies that the input/output current should be equal to the maximum rating (±20 mA), and that V_{CC} should also be not more than twice $V_{CC\,max}$ (14 V) for testing latch-up immunity with excess supply voltage. HCMOS ICs have been extensively subjected to the previously described tests with test parameters far exceeding those quoted by JEDEC. In no case did latch-up occur. For example, it has been determined that an HCMOS input can typically withstand continuous current (5s on, 15s off) of 100 mA to 120 mA, or 1 μs pulses of 300 mA with a duty factor or 0,001. An input can also withstand a discharge from a 200 pF capacitor charged to 330 V. An HCMOS output can withstand continuous current (5s on, 15s off) of 200 mA to 300 mA, or 1 μs pulses of 400 mA with a duty factor of 0,001. However, because there is an internal polysilicon 100 Ω resistor in series with all HCMOS inputs, the input voltages required to achieve these current levels are so high ($V_I = V_{CC} + 0{,}7\,V + 100I_I$) that it is unlikely that they could occur in practice, even in a 6 V system with severe glitches. Moreover, beyond these current levels, excessive heating occurs or aluminium tracks or bond wires break-down. It is therefore reasonable to conclude that HCMOS logic ICs are completely latch-up free.

THE LATCH-UP PHENOMENON

Output current triggered latch-up

A CMOS structure in which latch-up can occur is shown in Fig.1(a); the equivalent circuit formed by parasitic diodes of the n-channel MOS transistors with adjoining n^+ and p^+ regions is shown in Fig.1(b). The resistors represent resistance to lateral current flow and their values depend on circuit geometry and doping.

Application of a negative voltage to the output results in a current (I) which, in turn, gives rise to a current $I+(I/h_{FE})$ in the collector of TR_2. If this current causes sufficient voltage drop across r_c, TR_3 conducts. Since the h_{FE} of TR_2 is fairly high, hardly any of the collector current of TR_3 flows into the base of TR_2. Most of the collector current of TR_3 therefore flows through $r_{bb'1}$ and $r_{bb'2}$. If sufficient voltage is dropped across $r_{bb'1}$, TR_1 turns on. Since the collector current of TR_1 then further increases the base drive of TR_3, thyristor (SCR) TR_1/TR_3 is latched and current I, due to the negative voltage on the output pin, is no longer necessary to sustain the low impedance path between V_{CC} and ground. In principle, the current through SCR TR_1/TR_3 is only limited by the source resistance of the power supply.

Latch-up triggered by excessive supply voltage

Latch-up can also be initiated via the supply line. Figure 2(a) shows a similar circuit structure to that in Fig.1(a) but now TR_2 is lateral, formed by the source and drain junction of the associated n-channel MOS transistor forming part of a complementary inverter stage. Its p-channel complement (not shown), when conducting, connects the n-channel drain and the collector of TR_2 to V_{CC}. The equivalent circuit of this arrangement is in Fig.2(b).

Excessive supply voltage when the p-channel MOS transistor is conducting (output HIGH) can break-down the collector-base junction of TR_2. SCR TR_1/TR_3 will then be triggered if the resulting current-flow through $r_{bb'1}$ is sufficient to turn on TR_1. Although the breakdown current through TR_2 is limited by the on-state resistance of the p-channel MOS transistor, the current through SCR TR_1/TR_3 is limited only by power supply resistance.

It can be seen from Fig.2(b) that a fast positive-going transient on the supply line can also trigger SCR TR_1/TR_3 because it will cause current through $r_{bb'1}$ via the capacitance of the collector-base junction of TR_2.

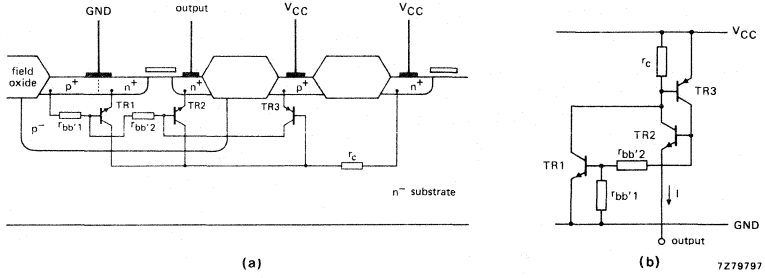


Fig.1 (a) Section through a CMOS IC showing how parasitic components are formed, (b) equivalent circuit of the parasitic components

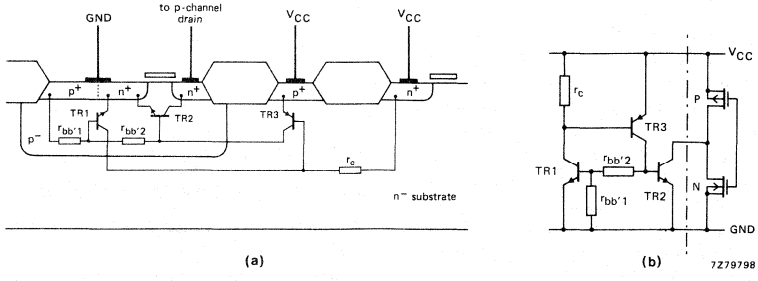


Fig.2 (a) The structure of Fig.1, but with TR_2 now formed laterally, (b) equivalent circuit incorporating lateral transistor TR_2

Input current triggered latch-up

As shown in Fig.3, all HCMOS ICs have an intentional input diode/resistor network to protect the thin oxide gate area of the logic against electrostatic discharges. If input voltages exceed V_{CC} by one V_{BE}, or go negative by more than one V_{BE}, current flows through the input diodes which, together with neighbouring diffusions on the die, can act as parts of parasitic bipolar structures such as transistors or 4-layer devices (SCRs).

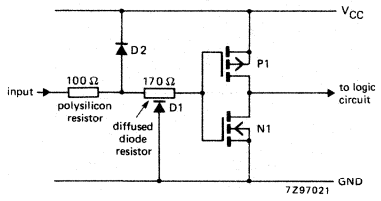


Fig.3 HCMOS input structure

WHY HCMOS LOGIC ICs ARE NOT LATCH-UP PRONE

It can be seen from Fig.1 and 2 that both the values of $r_{bb'1}$ and r_c, and the topologies of the p^+ and n^+ diffusions into the n-substrate are important factors influencing the susceptibility of a CMOS logic IC to thyristor latch-up. The latch-up immunity of HCMOS ICs has been considerably improved by careful design of the source-to-pocket contacts of the n-channel MOS transistors and the interchange of the p^+ and n^+ diffusions into the substrate as shown in Fig.4. The value of r_c could be reduced by arranging the n^+ diffusion as a guard ring around the n-channel MOS transistor but this would considerably increase the area of the device. As shown in Fig.5, the problem has been solved by preventing lateral current flow in the n^- substrate by growing an epitaxial layer on a very low resistivity substrate. Also important for improving latch-up immunity are the established HCMOS layout rules and process parameters that minimize the current gain of the parasitic bipolar transistors.

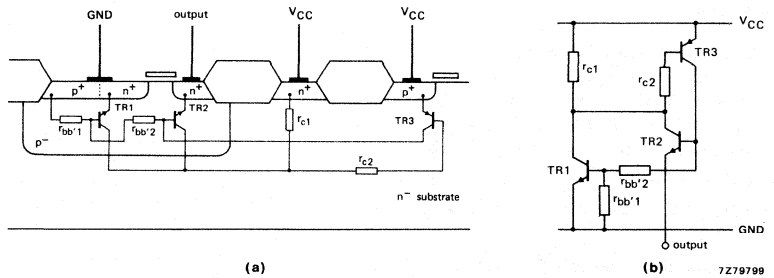


Fig.4 (a) Rearrangement of the structure of Fig.2 greatly increases latch-up immunity by incorporating base resistance r_{c2} (b) equivalent circuit

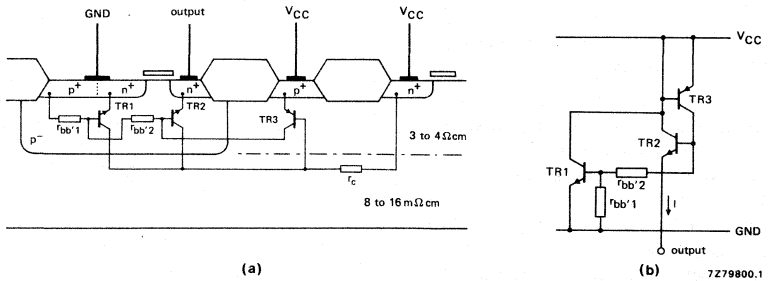


Fig.5 (a) By growing an epitaxial layer on a very low resistivity substrate, the lateral current flow responsible for latch-up is very largely eliminated, (b) equivalent circuit

LATCH-UP IMMUNITY TESTS

It should be noted that, when an HCMOS IC is subjected to a test to evaluate its immunity to latch-up, the applied currents and voltages will exceed the absolute maximum ratings of the IC to such an extent that they will almost certainly degrade its performance and may even destroy it. Latch-up immunity tests are therefore only intended for characterization purposes and should never from part of production tests. Any IC that has been subjected to latch-up immunity tests should be discarded so that it cannot be used for design or production purposes.

Test conditions and limits

When testing the immunity of HCMOS ICs to latch-up, the following limits and conditions must be observed:

- If $\pm I_I$ or $\pm I_O$ exceed the maximum ratings (±20 mA), the tests may be damaging or even destructive. For d.c. testing with higher currents, the trigger current should therefore only be applied for short periods (e.g. 5s) followed by a cooling period of three times this duration. Alternatively, automatic tests with low duty-factor pulsed current can be used.
- The minimum trigger current duration is 2 ms over the entire temperature range. The maximum trigger current duration is 5s. The rise and fall times are not critical but, to avoid correlation problems, suitable limits are 50 μs to 1 ms measured between the 10% and 90% amplitude points. A timing diagram is shown in Fig.8.
- The supply current (I_{CC}) must be limited to 200 mA to avoid excessive heating.
- Ambient temperature should be high (85 °C to 125 °C).
- To confirm that latch-up was the true cause of the quiescent supply current exceeding the maximum specified value after a latch-up immunity test, the IC must be checked electrically and functionally to verify that no damage has occurred.

Applying continuous (2 ms to 5s) input/output current to test latch-up immunity

Since the parasitic SCRs are current triggered, it is possible to trigger them by forcing current through the input protection diodes or through the parasitic bipolar structures at the output. The test circuit shown in Fig.6(a) forces current through the diode between an input/output pin and V_{CC}; the test circuit in Fig.6(b) forces current through the diode between an input/output pin and GND. The supply pin (V_{CC}) is at ground potential in Fig.6(a) because otherwise, the source of supply voltage would have to sink current and there would be danger of this causing the supply voltage to increase.

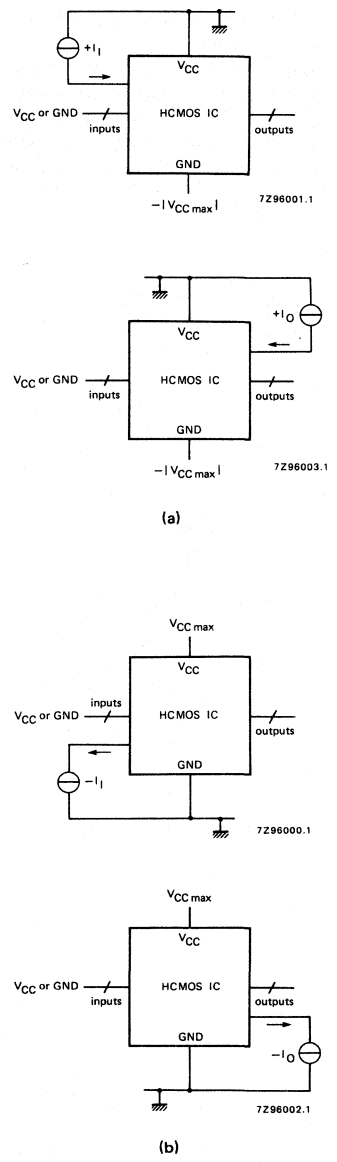


Fig.6 Latch-up immunity testing (a) positive input or output triggering, (b) negative input or output triggering

There are two methods of performing this test, the timing requirements for which are given in Fig.8. The first is to apply V_{CC} before forcing the current into the input/output. This simulates the application of an input/output voltage which exceeds the supply voltage. The test procedure is:

1. Connect all unused inputs of the IC under test to V_{CC} or GND.
2. Set the current source to zero.
3. Connect a current limited (200 mA max.) 7 V supply between the V_{CC} and GND pins of the IC under test.
4. Either ramp-up the current source or set it to the test level. If testing an output, make sure that the state of the IC inputs is such that the outputs is HIGH for positive-going trigger current, or LOW for negative-going trigger current. A 3-state output should be in the high impedance state.
5. Set the current source to zero and ensure that the input being tested is at V_{CC} or GND. If an output is being tested, check that it is open (current source disconnected).
6. Check the supply current (I_{CC}). If latch-up has occurred, it will be about 200 mA. If it is, verify that the input/output circuitry has not been damaged. This should not happen unless very high test currents have been used. If latch-up hasn't occurred (I_{CC} below max. specified value), test for continuity to determine whether the IC has been destroyed.

The second version of this test involves forcing the input/output currents before applying the supply voltage. This version therefore simulates a condition in which one section of a logic system is powered-down whilst its inputs remain active, and is then powered-up again. This could be caused by partial power failure or the plugging-in of boards without first switching-off (service engineers don't always follow the rules!). The test procedure is:

1. Connect all unused inputs to V_{CC} or GND.
2. Set the current source connected to the pin being tested to the test level. If testing an output, make sure that the state of the inputs is such that the output will be HIGH for positive-going trigger current, or LOW for negative-going trigger current. A 3-state output should be in the high-impedance state when the supply is connected.
3. Connect a current limited (200 mA max.) 7 V supply between the V_{CC} and GND pins of the IC under test.
4. Set the current source to zero and ensure that the input being tested is at V_{CC} or GND. If an output is being tested, check that it is open.
5. Check the supply current (I_{CC}) at V_{CC} = 6 V. If latch-up occurred, it will be about 200 mA. If it is, verify that the input/output circuitry has not been damaged. This should not happen unless very high test currents have been used. If latch-up hasn't occurred (I_{CC} below max. specified value), test for continuity to determine whether the IC has been destroyed.

We adopt this second version of the test as standard because we consider that it is more severe than the previous one. This is because, in the first test, the trigger current could be bypassed by the output circuitry when an output is being tested. Furthermore, the second version allows bench characterization using a curve tracer in the continuous writing mode so that the complete behaviour of the IC is displayed on the screen. For the first version of the test, the curve tracer would have to be in the d.c. mode and only dots would be displayed on its screen. Both versions of the test can be performed with automatic test equipment. Testing with a curve tracer is described in the Appendix.

Input voltage considerations

Although the parasitic SCRs in HCMOS ICs are current-triggered, the input/output voltage required to achieve the trigger current must also be considered.

As previously explained, all HCMOS ICs incorporate an input protection network which includes a 100 Ω polysilicon resistor in series with the input to limit current caused by excess input voltage (see Fig.3). This could occur due to ESD or failure of part of a power supply. Latch-up in a CMOS system is also an energy phenomenon because it can be caused by input signal overshoots or undershoots caused by crosstalk or flashes. The level of input current caused by this induced energy depends on the input voltage level. Since the polysilicon resistor in HCMOS IC inputs limits the input current, it is also necessary to consider the level of input voltage required to induce latch-up.

To force an input current of 100 mA through one of the input diodes via the polysilicon series resistor requires an input voltage of 100I + 0,7 V = 10,7 V beyond the limits V_{CC} and GND. Forcing such a high current into an HCMOS input to induce latch-up is therefore an unnecessarily severe test because the associated high input voltage is unlikely to occur in practice, even in a 6 V system with severe glitches or overshoots. Furthermore, as shown in Fig.7, forcing very high level currents into HCMOS inputs can destroy the input resistors. It should be noted that the energy (I^2Rt) in an input resistor increases fourfold each time the input current is doubled.

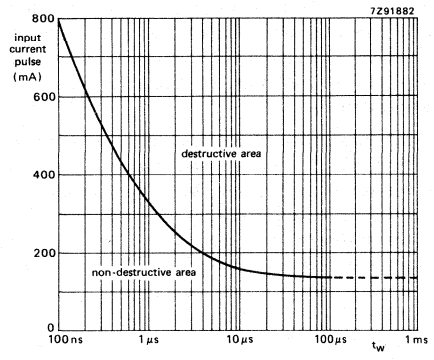


Fig.7 Destructive input current as a function of pulse width

Automatic testing of latch-up immunity

The previously described "continuous" current tests with timing as shown in Fig.8 are also suitable for automatic testing since most automatic testers incorporate current sources. Pulsed current testing with pulse widths much less than 2 ms has advantages over using longer duration pulses. For example:

- It more closely simulates glitches which are usually short-duration spikes.
- Less localized heating of the input structure allows the use of higher test currents. This is important because the ICs are less sensitive to lower currents. Latch-up is a bipolar phenomenon and requires the building up of storage effects. This effectively delays the start of SCR conduction so that higher current must be applied before latch-up occurs.

So, the main point to note is that, since the current is only applied for a short duration during an automatic test, the duration of the trigger current, and the interval between its removal and the measurement of V_{CC}, must be sufficient for latch-up, if any, to be established.

Figure 8(a) shows the timing for an automatic latch-up immunity test in which V_{CC} is applied before the input current is applied. Figure 8(b) shows the timing for an automatic latch-up test in which V_{CC} is applied after the input current has been established.

As with other modes of latch-up immunity testing, automatic testing can also damage the input structure if the test current exceeds the limits shown in Fig.7.

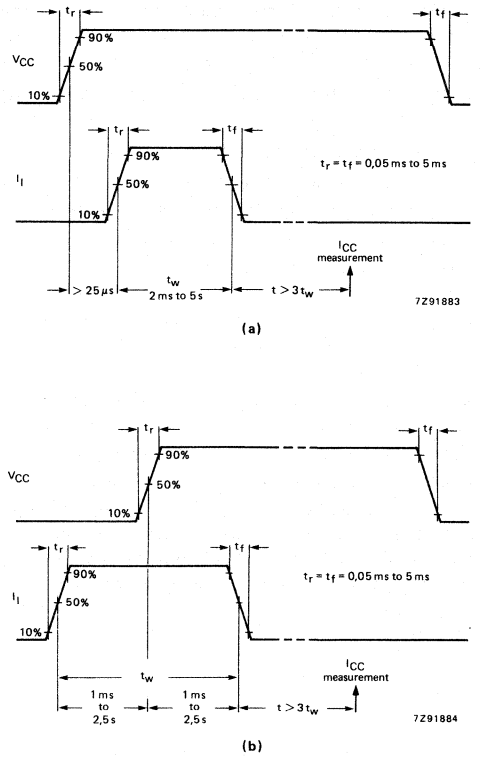


Fig.8 Timing for latch-up immunity tests (a) V_{CC} applied first, (b) I_I applied first. These timing diagrams only show positive-going currents and voltages but the timing for negative-going currents and voltages is the same

Testing latch-up immunity with simulated ESD at an input

It is also possible to initiate latch-up in a CMOS logic IC by inadvertantly applying a high-voltage electrostatic discharge (ESD) to its input (zapping). This can happen, for example, if an IC input is terminated with a connector or other fixture which is exposed to human touch. Such a situation can be simulated by discharging a pre-charged capacitor into the input using the test circuit in Fig.9(a) for a negative-going discharge, or the test circuit in Fig.9(b) for a positive-going discharge. The 1 MΩ resistors in the test circuits terminate the test input so that it doesn't float and cause erroneous results. The test procedure is:

1. Connect a 7 V supply (200 mA current limited) between the V_{CC} and GND pins of the IC under test.
2. Set the switch to charge the capacitor to the test voltage.
3. Switch the capacitor to the input.
4. After a few seconds, meaure I_{CC}. If it is greater than the maximum quiescent value quoted in the HCMOS family specification, latch-up has occurred.
5. Verify that any abnormal I_{CC} flow is not due to damage caused by the test.

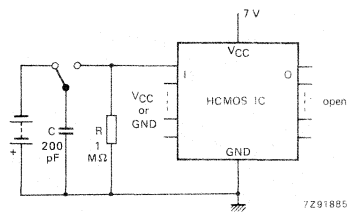


Fig.9 Latch-up immunity test for simulating ESD, (a) negative-going discharge, (b) positive-going discharge

Testing latch-up immunity with excess supply voltage

Latch-up can also occur if the supply voltage to an HCMOS logic IC increases beyond the absolute maximum rating to a level that causes the parasitic diode between the V_{CC} and GND rails to break down (20 V typical). Figure 10 shows that, if the supply current is limited to 100 mA, the supply voltage will then 'snap-back' to one of two holding voltages. If this voltage is above 7 V, the IC is immune to latch-up caused by excess supply voltage. If the holding voltage is below 7 V latch-up will have occurred. If excess supply voltage is applied to the IC for too long a period, the IC will be destroyed because the maximum power dissipated by it during the test will be as high as 2 W which is four times the maximum rating. The test procedure is:

1. Connect the test circuit as shown in Fig.11 with the supply current limited to 100 mA.
2. Increase V_{CC} until supply current flows.
3. Measure V_{CC}. If it is less than 7 V, latch-up has occurred.

This test can also be performed very rapidly by automatic testers or with a transistor curve tracer as described in the Appendix.

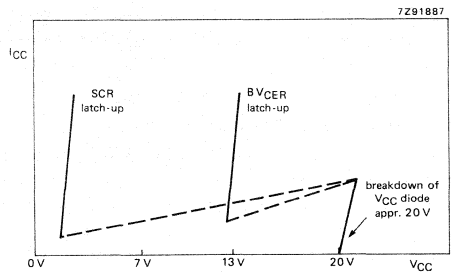


Fig.10 Sustaining voltages after testing for latch-up due to excess supply voltage

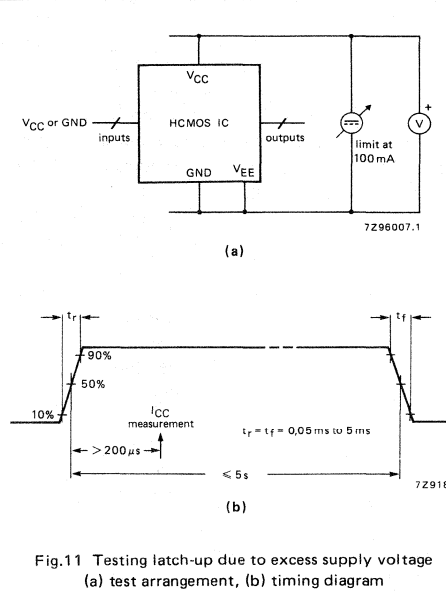


Fig.11 Testing latch-up due to excess supply voltage (a) test arrangement, (b) timing diagram

APPENDIX
LATCH-UP IMMUNITY TESTS USING A TRANSISTOR CURVE TRACER

The immunity of HCMOS ICs to latch-up caused by high input/output current or excessive supply voltage can also be evaluated with a transistor characteristic curve tracer such as the Tektronix 576. Using a curve tracer provides a quick and simple method of displaying the behaviour of the IC under test on a screen. If the correct value of collector resistor is selected in the curve tracer, the tests will be non-destructive and a wide range of currents can be used to stimulate latch-up. Any high supply current caused by input/output current can easily be observed. The collector resistor in the curve tracer influences the latch-up immunity tests in two ways:

1. It limits the supply current that can flow after latch-up, thereby making the tests non-destructive.
2. It has the undesirable effect of decreasing the supply voltage (V_{CC}) when supply current (I_{CC}) is flowing. To ensure minimum supply voltage reduction, the chosen value of collector resistor should therefore be as low as possible. However, to play safe, it is recommended that a fairly high value is selected for the collector resistor at the start of a test. The value can then be decreased whilst the effects of the tests are being observed on the screen of the curve tracer.

An important attribute of using a curve tracer is that it allows direct determination of any input current contribution to the supply current. Heating effects are also reduced because the collector voltage from the curve tracer is a continuous series of half sinewaves giving an average power dissipation of $(2/\pi)^2 V_{CC} I_{CC} = (V_{CC} I_{CC})/2{,}5$. When testing latch-up immunity with excess supply voltage, the V_{CC} diode breakdown voltage, secondary breakdown and the SCR effect can all be evaluated.

It is important to note that, to allow the latch-up phenomenon to be shown, all the curve tracer oscillograms presented in this Appendix show the results of tests on specially manufactured ICs which are much more prone to latch-up than the ICs of the 74HC/HCT/HCU family.

CURVE TRACER CHARACTERISTICS

Figure A1 shows the voltages and currents at the collector and base terminals of a transistor characteristic curve tracer. It can be seen that there is a continuous stepped current flow from the base terminal of the curve tracer into or out of the IC being tested. Since the level of the steps changes when the voltage at the collector terminal is zero, this is in accordance with the latch-up immunity test which calls for the input/output trigger current to be established before the supply voltage is applied. This is therefore a more severe form of test than one with a static supply voltage.

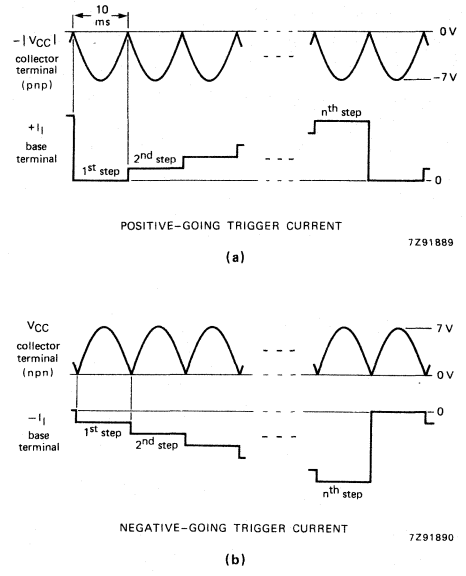


Fig.A1 Waveforms at the terminals of a transistor curve tracer

LATCH-UP IMMUNITY TESTS

Positive current into an input

The test arrangement is shown in Fig.6(a). The IC being tested should be connected to the curve tracer as follows:

- GND pin to the collector terminal.
- V_{CC} pin to the emitter terminal.
- Input pin to the base terminal (all unused inputs to GND or V_{CC}).

The controls of the curve tracer should be set as follows:

- Collector voltage: 15 V, pnp, normal mode.
- Collector series resistor: at least 140 Ω.
- Base current: 1 mA per step. Polarity: inverted.

The results of this test on a special IC used to demonstrate the latch-up phenomenon are shown in Fig.A2. The base line (top of oscillogram), being the zero current step, shows the leakage current ($-I_{GND}$) without input current. The increase of $-I_{GND}$ on the zero current step could be due to breakdown of a parasitic bipolar junction or the onset of a

field-effect leakage mechanism. According to the HCMOS specification, no supply current should flow with supply voltages up to 6 V. With higher supply voltage (even up to 15 V), 'leakage' increase can be observed by studying the zero current step trace. Because there is little parasitic bipolar action during the first three input current steps, there is very little $-I_{GND}$ flowing. The third current step (3 mA) results in I_{GND} of about 1 mA. This means that there is a bipolar transistor with a current gain of about 0,33 resulting in attenuation of about 3 in this testing mode. This will cause any positive input current to be attenuated about 3 times rather than being amplified. The fourth step (4 mA) results in the supply voltage falling to about 0,4 V due to SCR latch-up. The collector series resistor limits the supply current to about 45 mA (outside the picture). Any increase of current with V_{CC} greater than 7 V will be harmless because the maximum V_{CC} rating for HCMOS ICs is 7 V. However it does give an indication of how the IC will behave under severe stress or during high level V_{CC} transients.

This test can be varied by changing the combination of unused input connections and observing the screen to see if latch-up or early breakdown occurs. Especially to connect the input pins alternately to V_{CC} and GND or to apply an input combination such that as many as possible of the outputs are in the same logic state.

Negative current drawn from an input

The test arrangement is shown in Fig.6(b). The IC being tested should be connected to the curve tracer as follows:

- GND pin to the emitter terminal.
- V_{CC} pin to the collector terminal.
- Input pin to the base terminal (all unused inputs to V_{CC} or GND).

The controls of the curve tracer should be set as follows:

- Collector voltage: 15 V, npn, normal mode.
- Collector series resistor: at least 6,5 Ω.
- Base current: 10 mA per step. Polarity: inverted.

The results of this test on a special IC used to demonstrate the latch-up phenomenon are shown in Fig.A3. If only the input protection diode between the input pin and GND were forward biased, there would only be a current flow out of the GND pin. However, there is obviously also a parasitic npn transistor with its emitter connected to the input, its base connected to GND and its collector connected to V_{CC}. This diverts the input current to the V_{CC} pin. As can be seen, the first current step (10 mA) is completely diverted to the V_{CC} pin which means that the current gain between the input and V_{CC} pins is unity.

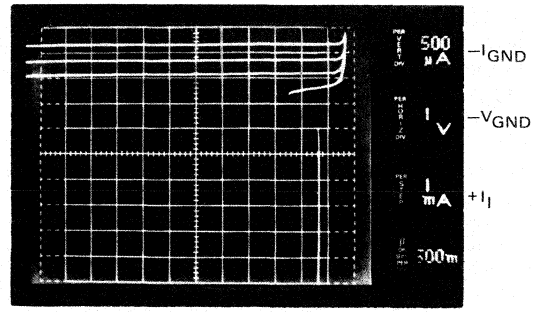


Fig.A2 Latch-up due to positive input current

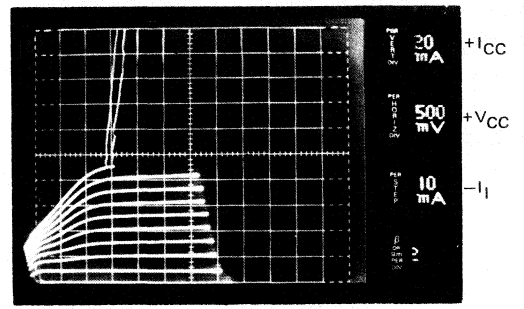


Fig.A3 Latch-up due to negative input current

A current at the V_{CC} pin which is much higher than that being drawn from the input pin would be undesirable because the excessive supply current could destroy the IC. The maximum acceptable current gain is 2 because 40 mA of input current would then cause a power dissipation of 240 mW at V_{CC} = 6 V. Latch-up occurs on the ninth input current step (90 mA).

Positive current into an output

The IC being tested should be connected to the curve tracer as follows:

- GND pin to the collector terminal.
- V_{CC} pin to the emitter terminal.
- Output pin to the base terminal (inputs set to cause HIGH output state or high impedance state for 3-state outputs).

The controls of the curve tracer should be set as follows:

- Collector voltage: 15 V, pnp, normal mode.
- Collector series resistor: at least 650 Ω.
- Base current: 5 mA per step. Polarity: inverted.

The results of this test on a special IC used to demonstrate the latch-up phenomenon are shown in Fig.A4. In this test the inherent pn output diode is forward biased. Forward-biasing the output diode before the supply voltage is applied is the most severe test because, if V_{CC} is present, the p-channel MOS output transistor will bypass the trigger current. The decrease of $-I_{GND}$ during the increase of V_{CC} in Fig.A4 is due to the conduction of the p-channel MOS output transistor as V_{CC} increases. Latch-up occurs on the sixth output current step (30 mA).

Negative current drawn from an output

The IC being tested should be connected to the curve tracer as follows:

- GND pin to the emitter terminal.
- V_{CC} pin to the collector terminal.
- Output pin to the base terminal (inputs set to cause LOW output state or high impedance state for 3-state outputs).

The controls of the curve tracer should be set as follows:

- Collector voltage: 15 V, npn, normal mode.
- Collector series resistor: at least 140 Ω.
- Base current: 10 mA per step. Polarity: inverted.

The results of this test on a special IC used to demonstrate the latch-up phenomenon are shown in Fig.A5. The inherent np output diode is forward biased and latch-up occurs on the third output current step (30 mA). Figure A5 also shows that negative output current causes current at the V_{CC} pin. If there is gain between the output and V_{CC} pins, undershoot at the output in will lead to additional supply current.

Excess supply voltage

This is a very simple test set-up which only uses the output from the collector terminal of the curve tracer. The IC being tested should be connected to the curve tracer as follows:

- GND pin to the emitter terminal.
- V_{CC} pin to the collector terminal.
- All input pins alternately to V_{CC} and GND.

The controls of the curve tracer should be set as follows:

- Collector voltage: 75 V, npn, normal mode.
- Collector series resistor: at least 650 Ω.

The results of this test on a special IC used to demonstrate the latch-up phenomenon are shown in Fig.A6. It can be seen that SCR latch-up occurs with only 750 microamps of supply current (I_{CC}) flowing. The sustaining voltage is as low as 1,5 V so the impedance between the supply pins is nearly zero.

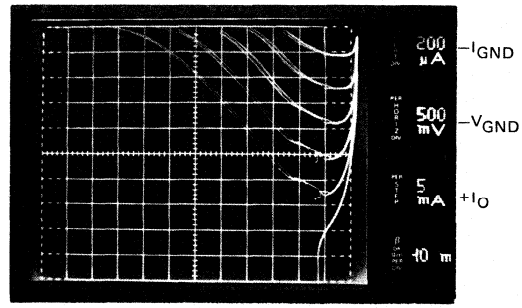


Fig.A4 Latch-up due to positive output current

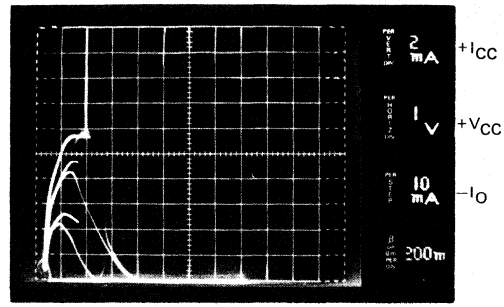


Fig.A5 Latch-up due to negative output current

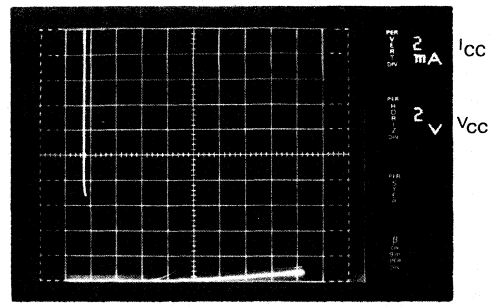


Fig.A6 Latch-up due to excess supply voltage

RESULTS OF LATCH-UP IMMUNITY ON HCMOS ICs USING A CURVE TRACER

The latch-up tests using a curve tracer have been extensively applied to 74HC/HCT/HCU logic ICs. In no case did latch-up occur. The input/output trigger tests were performed over the entire temperature range and used trigger currents up to ±100 mA continuous, and ±400 mA with a 100 ns pulse and a duty factor of 0,01. During the 100 mA continuous current test, excessive heating occurred, so the test time was restricted to a few seconds. During the test for latch-up with excess supply voltage, a breakdown current of 6,8 mA was necessary and the supply voltage snapped back to 12 V as shown in Fig.A7 in most cases. In no case was the sustain voltage less than 7 V.

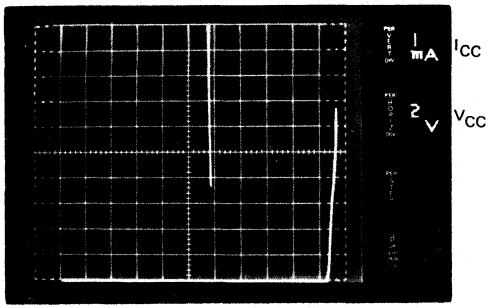


Fig.A7 Typical V_{CC} breakdown for HCMOS ICs occurs at V_{CC} = 21 V, I_{CC} = 6,8 mA.
The supply voltage then snaps back to 12 V

POWER DISSIPATION CONSIDERATIONS

For LSTTL logic ICs operating below 10 MHz, the most significant part of the total power dissipation is the quiescent power dissipation due to the many bipolar transistors that continuously conduct. With HCMOS logic ICs however, the converse is true because quiescent power dissipation is only due to leakage currents through reverse-biased junctions and is so low that it is practically negligible compared with the frequency-dependent dynamic power dissipation.

Since the logic functions in most systems only change state during brief periods, the average system frequency is between one and two orders of magnitude lower than the system clock frequency and the ICs therefore only draw quiescent current for most of the time. This means that replacing LSTTL ICs with equivalent 74HCT ICs, with their much lower quiescent power dissipation, results in a very significant reduction of overall system power dissipation without loss of operating speed.

However, total system power dissipation, is the sum of both the quiescent and the dynamic power dissipation of all the ICs and must be determined and minimized during system design. For LSTTL, where the quiescent power dissipation is the most significant contributor to the total power dissipation, the total power dissipation can be simply derived from the product of V_{CC} and I_{CC} given in the data sheets. For HCMOS circuits however, the dynamic power dissipation which is the most significant part of the total power dissipation is influenced by circuit design. It cannot be read direct from the data sheets but must be calculated from the supply voltage, average switching frequency, load capacitance, internal capacitances of the IC, and transient switching currents.

This article explains how our method of specifying HCMOS ICs in the data sheets makes it very simple to calculate their quiescent, dynamic and total power dissipation.

QUIESCENT POWER DISSIPATION

Quiescent power is dissipated by an IC when it is not switching and $V_I = V_{CC}$ or GND. Figure 1(a) will be used to illustrate this power dissipation in HCMOS ICs. In the quiescent state, either the PMOS or the NMOS transistor is fully off and, in theory, no direct MOS transistor channel path exists between V_{CC} and GND. In practice however, thermally generated minority charge-carriers, which are present in all reverse-biased diode junctions, allow a very small leakage current to flow between V_{CC} and GND. This quiescent supply current (I_{CC}) is specified in the published data.

Three factors influence the value of I_{CC}, and therefore the quiescent power dissipation, for a particular IC. They are:

Temperature: increasing temperature causes I_{CC} to increase because the minority charge-carriers in the reverse-biased diode junctions are thermally generated.

Device Complexity: MSI circuits dissipate more power than SSI circuits because they have a proportionally greater reverse-biased diode junction area.

Supply voltage: the number of minority charge-carriers is linearly related to reverse junction voltage.

Table 1 shows the JEDEC industry standard for the worst-case I_{CC} in HCMOS ICs. It shows the effect of temperature and circuit complexity on I_{CC} at the maximum recommended supply voltage V_{CC}. I_{CC} can be linearly derated for other supply voltages and would be approximately one-third of the value in Table 1 for a 74HC IC with $V_{CC} = 2$ V. Typical I_{CC} values are well below the maximum specified values.

TABLE 1
JEDEC industry standard for d.c. characteristics of HCMOS ICs
DC characteristics for 74HC/HCT

symbol	parameter	T_{amb} (°C) 74HC/HCT +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	unit	test conditions V_{CC} V *	V_I	other
	quiescent supply current											
I_{CC}	SSI	–	–	2,0		20,0	–	40,0	μA	5,5	V_{CC}	$I_O = 0$
I_{CC}	flip-flops	–	–	4,0		40,0	–	80,0	μA	5,5	or	$I_O = 0$
I_{CC}	MSI	–	–	8,0		80,0	–	160,0	μA	5,5	GND	$I_O = 0$

* for HC, $V_{CC} = 6$ V.

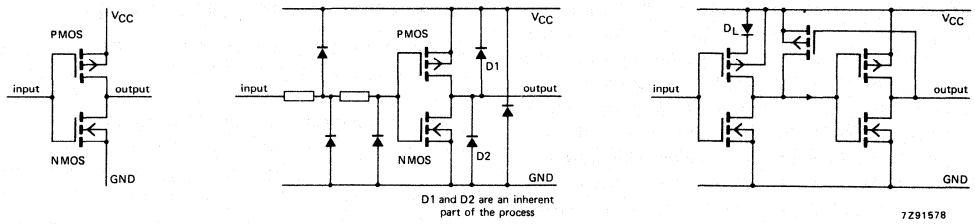


Fig.1 74HC inverter: (a) input structure of 74HC inverter; (b) 74HC inverter with protection circuitry; (c) input structure of 74HCT inverter

Another factor which influences quiescent power dissipation is the steady-state input voltage level which may slightly turn-on one of the input transistors shown in Fig.1(a) and yet not fully turn-off the other. This causes a small additional quiescent supply current (ΔI_{CC}) to flow between V_{CC} and GND. The level of ΔI_{CC} depends on the size of the input transistors and is different for each device.

In a system consisting entirely of 74HC ICs, the additional quiescent supply current ΔI_{CC} is so small that it can be omitted from practical power dissipation calculations. This is because 74HC outputs swing from GND to V_{CC}. The worst-case output levels with $|I_O| = 20\,\mu A$ are $V_{OL} = 0{,}1$ V max. and $V_{OH} = V_{CC} - 0{,}1$ V min., very close to GND and V_{CC} respectively. Figure 2(a) shows that ΔI_{CC} is negligible when these levels are applied to 74HC inputs because they always turn one of the input transistors fully off.

However, if 74HC input levels are held close to the switching threshold (typically $V_{CC}/2$), Fig.2 shows that the additional quiescent supply current (Δ_{CC}) becomes much greater than quiescent supply current I_{CC}. This occurs if the mistake is made of driving a 74HC input from a TTL output. With a minimum TTL V_{OH} of 2,4 V driving a 74HC input, not only will a logic "1" probably not be recognized, but several milliamps of (Δ_{CC}) will flow. To overcome this problem, an external pull-up resistor could be used as shown in Fig.3 but the resistor would dissipate significant power because its value would have to be low to maintain switching speed. 74HCT ICs have TTL input switching levels and should therefore be used instead of 74HC ICs whenever it is necessary to interface HCMOS with TTL logic.

Unlike 74HC ICs, 74HCT ICs can be substituted for LSTTL ICs and/or mixed with LSTTL, ALSTTL, ASTTL or FAST-TTL family ICs in the same system. Under some conditions, they may dissipate somewhat more quiescent power than 74HC ICs. For example, Fig.2(b) shows that a worst-case TTL V_{OL} of 0,5 V max. is close enough to GND

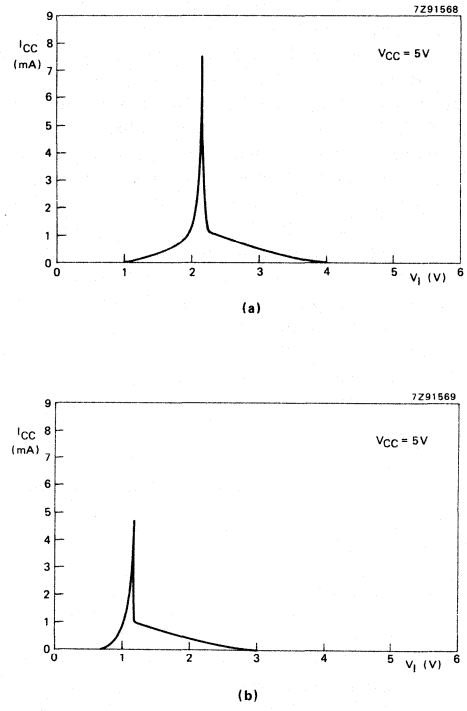


Fig.2 Supply current as a function of input voltage at $V_{CC} = 5$ V. (a) 74HC; (b) 74HCT

to turn the input NMOS transistor fully off so that ΔI_{CC} is close to zero. However, a worst-case TTL V_{OH} of 2,4 V min. causes some ΔI_{CC} to flow. For this reason, 74HCT data sheets specify I_{CC} at the worst-case input voltage of $V_{CC} - 2{,}1$ V for V_{CC} ranging from 4,5 V to 5,5 V. It is further specified on a per input pin basis to allow more accurate power dissipation calculations if all the functions within an IC are not being used, or are being driven by different input voltage levels.

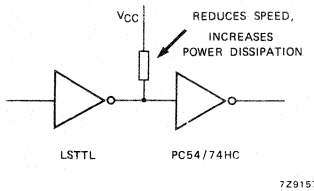


Fig.3 Using a pull-up resistor to interface 74HC ICs with LSTTL

Our proprietary 74HCT input structure shown in Fig.1(c) considerably reduces the additional quiescent supply current ΔI_{CC}. The structure is identical to that for 74HC circuits except for a level-shifting diode between the PMOS transistor and V_{CC}, and the connection of the substrate of the CMOS transistor to V_{CC}. The effect is to reduce the input level switching threshold to 28%V_{CC} instead of 50%V_{CC} as is the case with 74HC ICs. This therefore reduces the additional quiescent current ΔI_{CC} when a TTL minimum HIGH level of 2,4 V is applied to a 74HCT input by ensuring that the PMOS transistor is fully turned off. Figure 2(b) shows that ΔI_{CC} is negligible when a 74HCT input is held at a typical TTL HIGH output level (3,4 V) or LOW output level (0,25 V).

Calculating 74HC quiescent power dissipation

For power-critical applications such as battery-powered equipment, it may be necessary to calculate 74HC quiescent power dissipation as a standby value of battery drain. It is given by:

$$P_{QHC} = V_{CC} I_{CC} \qquad (1)$$

V_{CC} is dependent upon the particular application, we recommend that a ±10% variation be allowed. I_{CC} at V_{CCmax} is obtained from the data sheet for the particular IC. For critical battery-powered applications, the value of I_{CC} can be linearly derated for any desired V_{CC}; for example, at $V_{CC} = 2$ V, use one-third of the limits shown in Table 1 for 74HC ICs.

Calculating 74HCT quiescent power dissipation

Assume that an LSTTL IC with an output duty factor of 0,5 is switching one gate input in a 74HCT11 (triple 3-input AND gate) with a 5 V supply and an ambient temperature of 25 °C. Quiescent power dissipation is calculated from:

$$P_{QHCT} = V_{CC}(I_{CC} + \delta \Delta I_{CC}) \qquad (2)$$

where δ = switching duty factor.

ΔI_{CCmax} is calculated on a unit-load basis from the part of the data sheet reproduced in Table 2:

$\Delta I_{CCmax} = 360\,\mu$A per input pin x 1 pin x 0,5 unit-load coefficient = 180 μA.

Inserting this current and the values for V_{CC} (5,5 V), $I_{CC} = 2\,\mu$A from Table 2, and δ (0,5) into equation (2) gives:

$$P_{QHCT} = 5{,}5\text{ V } [2\,\mu\text{A} + (0{,}5 \times 180\,\mu\text{A})] = 506\,\mu\text{W}.$$

This is only 2% of the 25,5 mW maximum quiescent power that would be dissipated by the equivalent LSTTL IC. Furthermore, as previously stated, the ΔI_{CC} of 360 μA per input pin quoted in Table 2 for the 74HCT11 IC is based on a worst-case HIGH input level of $V_{CC} - 2{,}1$ V. In a typical application, the TTL HIGH input level driving the IC would be much higher than this, resulting in a reduction of ΔI_{CC} by an order of magnitude.

If all the inputs of a 74HCT IC are driven by 74HC or equivalent CMOS outputs, the input levels are such that the additional quiescent supply current ΔI_{CC} is so small that it can be omitted from 74HCT power dissipation calculations. 74HC quiescent power dissipation equation (1) can then be used to calculate 74HCT quiescent power dissipation.

DYNAMIC POWER DISSIPATION

Unlike quiescent power dissipation, dynamic power dissipation is calculated in the same manner for both 74HC and 74HCT ICs. All equations presented here for dynamic power dissipation are therefore applicable to both 74HC and 74HCT ICs.

Three factors influence the dynamic power dissipation of HCMOS ICs. They are load capacitance, internal capacitance and switching transient currents (through-currents of transistor pairs when both transistors momentarily conduct during logic level transitions).

TABLE 2
Specification of I_{CC}, ΔI_{CC} and unit load coefficient for 74HCT11 triple 3-input AND gate

symbol	parameter	T_{amb} (°C) 74HCT +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	unit	test conditions V_{CC} V	V_I	other
I_{CC}	quiescent supply current			2,0		20,0		40,0	μA	5,5	V_{CC} or GND	$I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4,5 to 5,5	V_{CC} −2,1 V	other inputs at V_{CC} or GND: $I_O = 0$

Note:

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in table below.

input	unit load coefficient
nA, nB, nC	0,5

Load capacitance

The first contribution to dynamic power dissipation is caused by the charging and discharging of external capacitive loads. Figure 4 illustrates an HCMOS inverter with a capacitive load and, together with the following equations, will help to illustrate how load capacitance consumes power. The energy dissipated (joules) in charging and discharging the capacitive load is:

$$P_{CL}t = C_L V_{CC}^2 \quad (3)$$

where $t = 1/f_o$ and C_L = total external load capacitance due to interconnections, driven inputs and any sockets that are used.

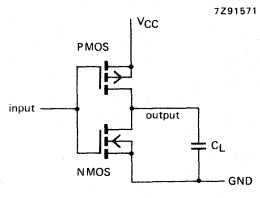


Fig.4 74HC inverter driving a capacitive load

The dynamic power dissipation due to capacitive loads is therefore:

$$P_{CL} = C_L V_{CC}^2 f_o \quad (4)$$

Equation (4) is only applicable if all the outputs are switching the same load. If they are not, the equation becomes:

$$P_{CL} = \Sigma(C_L V_{CC}^2 f_o) \quad (5)$$

For multiple output ICs, it is important to calculate with the appropriate output frequency. For example, at either output from a flip-flop, $f_o = f_i/2$; for a 7-stage binary ripple counter (type 74HC/HCT4024), f_o is halved for each successive output stage so that $f_o = f_i/64$ for the final output stage.

Internal capacitance

All MOS logic ICs have internal parasitic capacitance caused by diode junctions, MOS transistor structures, and the aluminium and polysilicon interconnections. It has the same effect as external capacitive loads, and its magnitude depends on the complexity of the circuit.

HCMOS ICs are manufactured with a self-aligned polysilicon gate process (3 μm gate length) and local oxidation to reduce internal capacitance by minimising gate-to-source

and gate-to-drain capacitances. The junction capacitances, which are proportional to junction area, are smaller than those in HE4000B CMOS ICs because the diffusions are shallower. Figure 5 shows the location of the capacitances in a 74HC inverter.

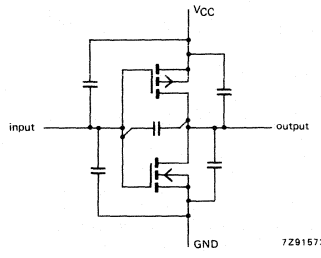


Fig.5 Location of capacitances in a 74HC inverter

For power dissipation calculation purposes, the total load caused by internal capacitances and by switching transient currents is defined as a single effective internal no-load power dissipation capacitance C_{PD}. It is defined in the data sheet for each HCMOS IC on a 'per function' basis and, where appropriate, it is also separately specified for each different logic function (e.g. gate or flip-flop) within an IC. This allows more accurate power dissipation calculations to be made if logic functions within the same IC are operating at different frequencies.

The published figure for C_{PD} is valid for the worst-case operating mode under typical operating conditions. For example, in the case of a NAND gate, the state of the inputs is assumed to be such that the output is changing state; for a shift register or D-type flip-flop, it is assumed that alternately HIGH/LOW data is being clocked in. The specified value for C_{PD} however is a typical one; nevertheless, some protection will already be built-in to dynamic power dissipation calculations because the assumed worst-case operating modes don't always occur. Although we're not yet prepared to officially publish a maximum value for C_{PD}, a rough guide would be to increase the published figure by 50% for worst-case calculations. The method of measuring C_{PD} is explained in the chapter "User Guide".

Switching transient currents

The final factor that contributes to the dynamic power dissipation of HCMOS is internal switching transient currents. When the output of a basic HCMOS inverter as shown in Fig.6(a) changes state, either from a logic "1" to a logic "0" or vice-versa, there is a brief period during which both transistors conduct. This creates a temporary low-resistance path between V_{CC} and GND as shown in Fig.6(b). In this transistory state, additional supply current (ΔI_{CC}) flows and power is dissipated, so input rise and fall times should be kept short. The average value of this transient current increases linearly with increasing switching frequency. In other words, power dissipation due to switching (like power dissipation due to internal capacitance) increases linearly with increasing switching frequency. However, since it is small compared to the power dissipation due to internal capacitance, its effect is included in the published value of power dissipation capacitance (C_{PD}) which has discussed under the previous heading.

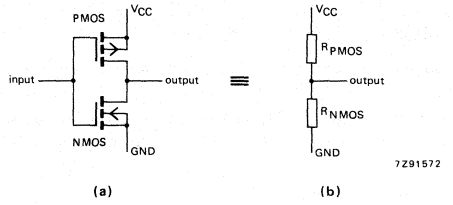


Fig.6 When an HCMOS inverter changes state, both input transistors momentarily conduct: (a) inverter input structure; (b) equivalent circuit when the input level is between logic levels

Total dynamic power dissipation

Since C_{PD} represents the load imposed by both internal capacitance and switching transient currents, the total dynamic power dissipation due to these factors is:

$$P_{DYN} = C_{PD}V_{CC}^2f_i \quad (6)$$

The total dynamic power dissipation of HCMOS ICs is obtained by adding equation (6) to the power dissipation due to the total external capacitive load (equation 5) and is given by:

$$P_D = C_{PD}V_{CC}^2f_i + \Sigma\,(C_LV_{CC}^2f_o) \quad (7)$$

CALCULATING TOTAL POWER DISSIPATION FOR 74HC AND 74HCT ICs

Total HCMOS power dissipation is a summation of the appropriate quiescent and dynamic power dissipation formulae previously described.

For 74HC/HCT ICs driven by CMOS levels:

$$P_{tot} = V_{CC}I_{CC} + C_{PD}V_{CC}^2f_i + \Sigma\,(C_LV_{CC}^2f_o) \quad (8)$$

For 74HCT ICs driven by TTL:

$$P_{tot} = V_{CC}(I_{CC} + \delta\Delta I_{CC}) + C_{PD}V_{CC}^2f_i + \Sigma\,(C_LV_{CC}^2f_o) \quad (9)$$

POWER DISSIPATION IN OSCILLATORS AND ONE-SHOTS

The information presented so far is only valid for ICs switching rapidly between logic levels. Additional quiescent supply current ΔI_{CC} is greater for one-shots, oscillators and gates arranged as oscillators because, in these applications, the input slowly passes through the switching threshold (typically 50%V_{CC} for 74HC ICs and 28%V_{CC} for 74HCT ICs) causing flow-through current as shown in Fig.2.

POWER DISSIPATION COMPARISON BETWEEN HCMOS, LSTTL AND ALSTTL

In any IC, there is a balance between speed and power dissipation. LSTTL logic is relatively fast but the quiescent power dissipated by its bipolar circuitry is considerable. ALSTTL improves upon LSTTL by using advanced wafer fabrication techniques and smaller geometries. These improvements increase speed and approximately halve the quiescent power dissipation.

CMOS ICs dissipate negligible quiescent power compared with all bipolar TTL logic ICs but, until the development of the HCMOS family, CMOS ICs were relatively slow. Use of advanced wafer fabrication techniques and smaller geometries has now made it possible for HCMOS to match the speed of LSTTL and yet retain the substantial power savings afforded by CMOS. Figure 7 shows the speed-power products for today's most popular logic IC technologies.

Figures 8 and 9 compare the dynamic power dissipation of SSI and MSI for 74HC, and LSTTL ICs. These graphs show that 74HC ICs maintain their power dissipation advantages for switching frequencies up to several MHz. This is because power is only dissipated during switching. The constant, frequency-independent power dissipation exhibited by LSTTL ICs is caused by the many bipolar transistors that continuously conduct.

Figures 8 and 9 also show that, as device complexity increases, the frequency at which HCMOS ICs dissipate the same amount of power as LSTTL ICs also increases. This is because, as LSTTL complexity increases, there are more resistive paths between V_{CC} and GND which carry more quiescent bias current and thus cause more quiescent power dissipation. HCMOS ICs also dissipate more quiescent power as their complexity increases, but the leakage currents which cause it are so small that it can be ignored.

The power dissipation of the different logic IC technologies is translated into total system power as a function of frequency in Fig.10 which is for a small system consisting of one gate and two flip-flops. The graph shows that HCMOS also dissipates substantially less power than LSTTL at the system level.

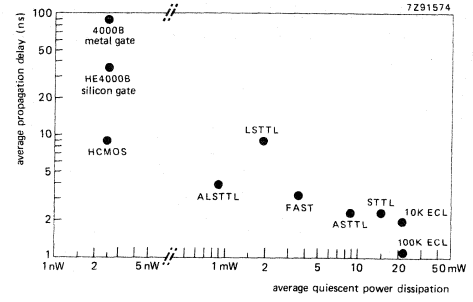


Fig.7 Speed/power products for the most popular logic IC technologies

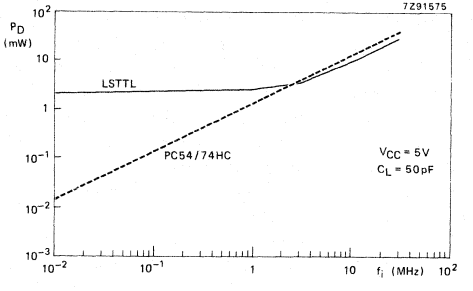


Fig.8 Total power dissipation as a function of switching frequency for gates

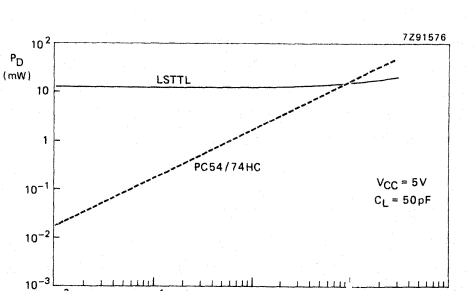


Fig.9 Total power dissipation as a function of frequency for a dual flip-flop with one of the flip-flops toggling

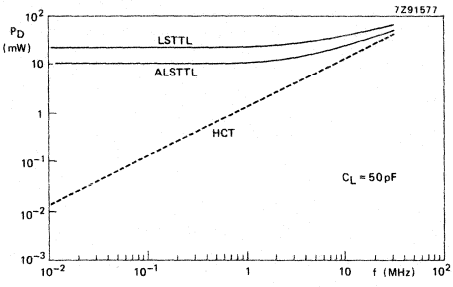


Fig.10 Total power dissipation as a function of frequency for a small system comprising one gate and two flip-flops

INFLUENCE OF HCMOS ICs ON APPLICATIONS

The significantly lower power dissipation in an HCMOS logic system, compared with its LSTTL or ALSTTL equivalent, is *the* primary reason why HCMOS ICs should be used for new system designs and to replace LSTTL or ALSTTL ICs in many existing designs where power consumption and/or dissipation is a problem.

For new designs, HCMOS is the only suitable family of logic ICs for battery-powered portable personal computers. The use of HCMOS is *the* major trend in personal computers using all CMOS microprocessors, RAMs, ROMs, and peripherals. All CMOS designs can be powered-down to 2 V standby to extend battery life.

For non-portable equipment, the use of HCMOS logic and CMOS LSI is also preferred because it not only reduces power dissipation, but also significantly reduces, in order of priority, cost, size, and weight. Cost reductions stem from major reductions of power supply current and regulation, cooling fans, heatsinks, and copper buses.

An equally powerful motivating force for using HCMOS logic ICs with their lower power dissipation is the inherent and proven increase of component and equipment reliability. Equipment life is considerably extended because IC junction temperatures are much reduced and other components are exposed to lower ambient temperatures.

POWER SUPPLY LINE LAYOUT AND DECOUPLING RECOMMENDATIONS

Spikes due to output current switching and the charging and discharging of parasitic capacitance, are the two main sources of noise on the power lines of HCMOS logic systems. To minimize noise, the power supply should be decoupled. However, if switching speed is high, not only the voltage dips on the power lines must be considered but also the effects of di/dt radiation. Decoupling requirements are a balance between the precautions necessary to reduce the effects of these two phenomena.

The first requirement for minimizing noise is a well designed power distribution network. For instance, it is essential to have a good ground (GND) connection pattern on a pcb. Even the commonly used GND pattern shown in Fig.1 can cause problems. In Fig.1, an output from IC1 drives an input of IC2, and an output from IC3 drives an input of IC4. Since the signal paths between IC1 and IC2, and between IC3 and IC4 are not coupled, there should be no crosstalk between them. However, IC1 and IC3 share the hatched section of the GND comb, and, when the output of IC1 switches, a spike could be generated on the GND of IC3. This could be transmitted to IC4 via the IC3-IC4 signal connection causing the output of IC4 to switch erroneously. If a double-sided board is used, it is therefore advisable to reduce the length of individual sections of the GND comb by installing links on the opposite side of the board as shown in Fig.2. This is especially important for boards on which high level currents are switched.

It is bad practice to use jumpers to connect GND/V_{CC} pins of ICs to pcb tracks (Fig.3). Jumpers are unlikely to be used on production boards, but they should not be used on prototype or one-off boards either because the inductance they introduce into the lines causes coupling between outputs. Printed connections should therefore be used to interconnect power tracks and IC pins. An even better solution is to use multi-layer boards so that individual layers can be used as a V_{CC} plane and a groundplane. The power supply can then be connected directly to the IC supply pins. Also, the inherent capacitance between the V_{CC} plane and the groundplane will reduce the amplitude of any high frequency noise on the power supply.

This inherent capacitance has the distinct advantage of being free from the inductance associated with discrete decoupling capacitors. A less expensive alternative to a multi-layer board is a multi-wire board which offers the same high frequency noise characteristics. With double-sided boards, it is not possible to dedicate a layer to a V_{CC} plane and a groundplane. Nevertheless, if at all possible, it is still best to have the V_{CC} and ground tracks on opposite sides of the board.

Connectors on any type of pcb should each have at least five ground pins to obtain good distribution of ground current.

The precautions outlined for ground tracks on the pcb are equally applicable to the power (V_{CC}) lines.

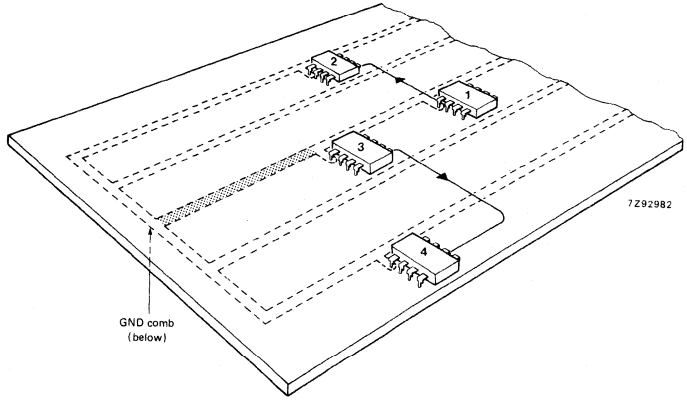


Fig.1 Common ground path on double-sided board

The wide HCMOS power supply range of 2 V to 6 V may suggest that voltage regulation is not necessary, but it must be remembered that supply voltage level variations will influence switching speed, noise immunity and power consumption. Supply voltage differences between ICs must also be avoided because a difference of as little as 0,5 V between power lines can cause unwanted effects. To isolate noise sources and avoid the use of a large voltage stabilizer with its heavy gauge (low impedance) wiring to each board, it is better to have a separate stabilizer for each board. However, care must be taken because a fault on a stabilizer for one board may be transmitted via the HCMOS input structure to other boards, possibly causing damage.

No matter how good the V_{CC} and GND connections are, all line inductance cannot be eliminated. This is where decoupling plays its part.

Ceramic capacitors are best for decoupling because they have very low series inductance. The advantage of using them will, however, be lost if they are connected too far from the IC. The inductance of the long tracks in conjunction with the capacitor will then form a very high-Q LC tuned-circuit, and the oscillations produced will have a worse effect than not having any decoupling at all. If it is impossible to make connections between decoupling capacitors and ICs shorter than 20 mm, then use several tracks connected in parallel and separated by at least one track-width (Fig.4). Some ceramic capacitors have preformed leads as shown in Fig.5(a). These leads introduce unwanted inductance. It is better to use capacitors with straight leads mounted as shown in Fig.5(b).

In general, the minimum requirements for good decoupling are:

- one 47 μF bulk capacitor per Eurocard
- one 1 μF tantalum capacitor per 10 packages of SSI logic
- one 22 nF ceramic capacitor for each octal IC and for each counter/shift register (MSI logic)
- one 22 nF ceramic capacitor per 4 packages of SSI logic

An example showing how to determine the value of decoupling capacitor follows. Assume a buffer output sees a 100 Ω dynamic load and the output LOW-to-HIGH transition is 5 V; the current demand is therefore 50 mA per output. For an octal buffer, the current demand would be 0,4 A for 6 ns.

The instantaneous current in the capacitor is:

$$i = \frac{\Delta Q}{\Delta t}$$

$$\text{And } i = \frac{C\Delta V}{\Delta t} \quad (\text{from } Q = CV)$$

$$\text{Therefore, } C = \frac{i\Delta t}{\Delta V}$$

For an octal buffer and a change in V_{CC} of 0,4 V say,

$$C = \frac{0{,}4\ \text{A} \times 6 \times 10^{-9}\ \text{ns}}{0{,}4\ \text{V}} = 6\ \text{nF}.$$

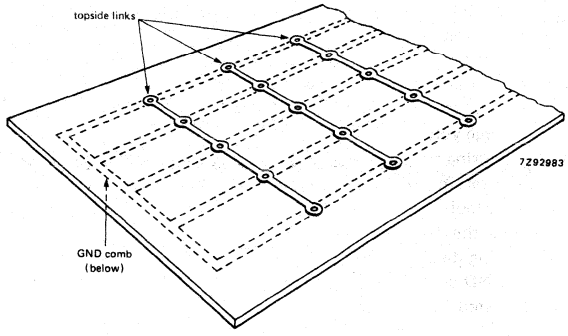


Fig.2 Reducing the length of common ground paths on double-sided board

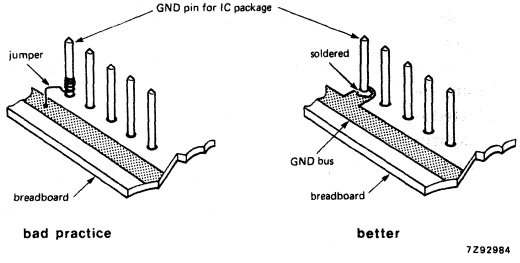


Fig.3 Methods of making ground connections

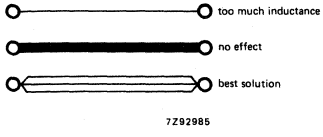


Fig.4 Power supply tracks

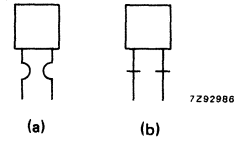


Fig.5 Leads of decoupling capacitors:
(a)unsuitable; (b) preferred

BATTERY BACK-UP OF HCMOS LOGIC ICs

HCMOS logic ICs, in contrast to other logic families, can easily be provided with battery backup in the event of failure of the normal power supply. Two of the main reasons for this are their very low quiescent power consumption (quiescent currents typically in the low nA region compared with around 2 mA for LSTTL ICs), and their fast transition time, which minimize the time they spend in the linear region and hence the power they consume during switching. Added to these is the fact that HCMOS ICs operate quite happily at supply voltages significantly lower than their nominal supply voltage (say as low as 2 V compared with a minimum of 4,75 V for LSTTL), so except for a reduction in speed, a 2 V battery supply voltage is no hindrance to efficient operation.

For long periods of battery operation, however, there are a number of simple guidelines you should follow. None are essential, but if you stick to them you will at least minimize power consumption and assure maximum battery life.

MINIMIZING POWER CONSUMPTION IN BATTERY-BACKED SYSTEMS

Don't use non-CMOS circuitry

Avoid using non-CMOS circuits in your design, this includes microprocessors and memories, otherwise you'll incur the inevitable penalty of higher power consumption. Remember, non-CMOS circuits draw quiescent supply currents that are often too high for battery operation. And although you can provide non-CMOS sections of your circuits with facilities for reduced-power (and hence slower) operation or for a completely idle power-down mode (for data retention only), in both these cases you'll find that operation of battery-backed up sections is likely to suffer severely in the event of a power failure. With all-CMOS circuitry, you won't have these problems at all.

Aim at low-frequency operation

Aim at low-frequency operation or switch logic ICs to the idle state if operation is not required. In CMOS systems, the dynamic power dissipation P_D is one of the greatest sources of power loss (static supply current drawn by CMOS circuits being almost negligible) and this is related to the input and output frequencies f_i and f_o by:

$$P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) \qquad (1)$$

in which V_{CC} is the supply voltage, C_{PD} is the power-dissipation capacitance per device (obtainable from the data sheets) and C_L is the output load capacitance. P_D therefore varies directly with operating frequency.

An example should illustrate this. A typical MSI circuit with two outputs loaded with 50 pF will have a total load capacitance ($C_{PD} + 2C_L$) of 150 pF. Even with an operating frequency as low as 15 kHz, this will result in a dynamic supply current of 14 μA (with a 5 V supply), almost double the maximum quiescent supply current of 8 μA. And since operating frequencies may often be several orders of magnitude greater than this, you can appreciate how significant dynamic power dissipation can be, and how important it is to keep your operating frequency as low as possible.

The alternative is to add extra circuitry such as multiplexers to reduce overall power consumption. Multiplexers direct the information bit streams only to sections where they are needed, and allow all unused logic to be switched to the idle state in which it dissipates (negligible) leakage current only.

Use low-value capacitors to minimize charging losses

From the above discussion you can see that dynamic power dissipation is also proportional to load capacitance, so if capacitors are needed, make sure their values are as low as possible to minimize charging energy losses. High value load capacitance also increase transition times and hence the time the inputs spend in the linear region (see next item).

Make sure transitions are fast

The longer the voltage level of an input waveform is maintained between the undefined logic region of the MOS transistors (the linear region), the longer both the n-and p-channel input transistors remain conducting and the greater the power dissipation. Maximum current through the transistors (through-current) occurs at 50% of V_{CC} for 74HC ICs and at 28% of V_{CC} for 74HCT ICs, but there will also be significant current throughout the linear region, i.e. for V_I between $V_{IL\,max}$ and $V_{CC} - V_{IH\,min}$, which for a V_{CC} of 4,5 V means V_I between 1,35 V and 3,15 V. So you can see that input waveforms play a significant role in determining power loss.

Usually output rise/fall times and hence input rise/fall times of 20 ns at 5 V or 60 ns at 3 V are satisfactory to minimize power loss due to through-current.

When an output is heavily loaded capacitively and its signal is distributed to many inputs, the waveform can be squared-up (i.e. the capacitance reduced) by splitting the line at the output into several sections and driving these sections with independent drivers.

Finally, there's a common misconception that Schmitt triggers draw little through-current in the linear region.

Whilst it's certainly true that the output transitions of a Schmitt trigger are fast, there's no guarantee that the input transitions will be. Indeed, since Schmitt triggers are generally used to square-up slow waveforms, there's a very good chance that input transitions will be slow and that heavy through currents will be drawn. The data sheets give you the through-currents drawn by Schmitt triggers.

This through-current phenomenon is adequately described in the User Guide Section, but you can get a rough idea of the through-current drawn by a 74HC IC for a given input voltage by looking at the unit load coefficient of its 74HCT counterpart. The unit load coefficient of a 74HCT IC is an indication of the size of the input transistors and hence of the current they consume during transitions. A type with a unit load coefficient of say 0,3, will draw only 0,3 times the through-current of a type with a unit load coefficient of one. So you can calculate the through-current drawn by a 74HCT IC for a given input voltage by multiplying its unit load coefficient by the current given in the through-current graph in the User Guide. And since nearly all 74HC and their 74HCT counterparts are produced by similar aluminium interconnect masks, this will give you an indication of which 74HC types draw the lowest through-current for the input voltage you want to operate at.

Avoid the use of pull-up resistors

Don't use input or output pull-up resistors at the interface between the high-power (mains) fed section and the battery-fed section, since they can lead to sneak current paths when the normal power supply fails.

Although any pull-up or pull-down resistor disspates power, an input pull-up resistor that's returned to the V_{CC} rail of the battery-fed section will create a current sneak path when the high-power section fails (Fig.1). If resistors are necessary, use the highest values possible e.g. 1 MΩ.

If you look at Fig.1, you'll see that the sneak current path travels through the pull-up resistor R_{PU}, back along the signal path to the higher power logic, and forward-biases the input or output CMOS protection diodes (or the protection diodes in TTL), and supplies current to the high-power logic, severely draining the back-up battery.

Figure 2 shows how you can instead select a pull-down resistor (R_{PD}) that avoids this problem.

The minimum value of R_{PD} is selected to guarantee that the HIGH output level of the driver doesn't fall below the $V_{OH\,min}$ for the $I_{OH\,min}$ being sourced. In Fig.2, resistor R_{on} represents the "on" resistance of the p-channel transistor of the driver IC. Its value is given by:

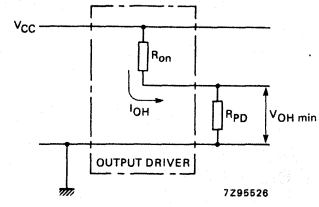


Fig.2 Pull-down resistors avoid the problems of sneak current paths. The minimum value of the pull-down resistance R_{PD} must be selected to guarantee that the HIGH output level of the driver doesn't fall below the $V_{OH\,min}$ for the $I_{OH\,min}$ being sourced. R_{on} represents the on resistance of the p-channel transistor of the driver IC

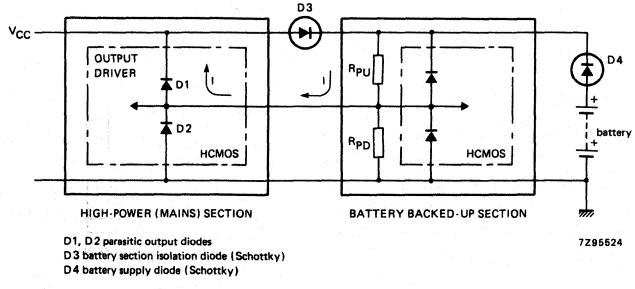


Fig.1 Pull-up resistors at the interface between high-power (mains) fed sections and the battery-fed section can lead to a sneak currents (I) when the normal power supply fails. This current passes through the pull-up resistor R_{PU}, back along the signal path to the high-power logic, severely draining the back-up battery

$$R_{on} = \frac{V_{CC} - V_{OH}}{I_{OH}}$$

and the value of $R_{PD\,min}$ is given by:

$$R_{PD\,min} = \frac{V_{OH\,min}}{I_{OH\,min}}$$

Example:

For $V_{CC} = 4{,}5$ V, $V_{OH\,min} = 3{,}98$ V at $I_{OH\,min} = 4$ mA and:

$$R_{PD\,min} = 3{,}98/(4 \times 10^{-3}) \simeq 1\,k\Omega.$$

The maximum value of R_{PD} is set by the maximum allowable leakage current that will still allow the logic to reach its required level. For supply voltages lower than 4,5 V, use the output curves in the User Guide to determine the output current available.

Pull-up resistors should also be avoided on buses at the interface between battery backed-up sections and high-power sections, and you should design the system with active-HIGH signals at the bus. Then when power fails, the outputs of the high-power section will be set to their initial state. If instead you opted for active-LOW signals at the bus, you would again get a current sneak path through the protection diodes of the high-power section (Fig.3), severely draining the back-up battery.

Use the minimum supply voltage for your needs

From expression (1), you can see that dynamic power dissipation is also proportional to the square of the supply voltage. So for the battery-fed section, at least, it's essential to keep the supply voltage low. You should, in fact, choose a supply voltage just high enough to fulfil your speed requirements.

It's worth mentioning here the new low-voltage Jedec Standard 8 for battery operated systems. This standard was established to allow for future scaling-down of design rules without the problems caused by high electric-field stresses that would inevitably occur if the supply were to remain at 5 V. The Standard recognizes the need to maintain compatability with existing 5 V TTL circuitry, and accordingly, recommends somewhat higher operating voltages than would be expected purely on the basis of directly scaling down of design rules.

The recommended voltages are 3,3 V ± 0,3 V for the normal power supply and 2,8 V ± 0,8 V for unregulated LVBO (low-voltage battery operation). These are, of course, ideal for HCMOS, but designers must be able to contend with the nearly ±30% voltage fluctuation the standard allows for battery powered systems (which provides a 2 V lower limit covering the end-of-discharge levels of lead-acid cells and two series-connected nickel-cadmium cells, as well as of lithium-based cells). Standard 8 also specifies the d.c. interface parameters that provide for inter-system compatability between the LVBO HCMOS and TTL.

Use only low-power LCDs

If you are using LCDs, make sure they are low-power ones. And remember, since no quiescent current flows in an LCD, make sure you also use low-capacitance versions.

Power-down microprocessors and memories when not in use

Power-down microprocessors and memories when not in use and switch logic to its idle state when operation is not required.

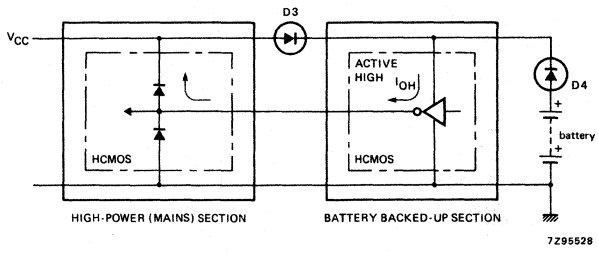


Fig.3 Systems should be designed with active-HIGH signals at buses interfacing battery backed-up sections and high-power sections. This again avoids current sneak paths and sets outputs of the high-power sections to their initials state when power fails

Here, you will probably have to devise software or hardware controlled stand-by facilities to yield power savings when (long) battery operation is required. Remember that systems generally spend most of their time waiting for external events to occur or for specified intervals to elapse, so design your software to take advantage of this fact. Remember also that memories spend most of their time in the quiescent mode, so you should use memory ICs that consume minimum power in this mode. Here, of course, you'll find CMOS systems ideal. Finally, minimize switching by basing your designs on algorithms that reduce the number of gates which have to switch to perform a particular function. Silencing unused logic is another way to eliminate unnecessary gate switching.

Terminate unused inputs

Terminate all unused inputs, either to V_{CC} or to GND (via resistors of between 1 kΩ and 1 MΩ), otherwise you might find some inputs floating into the linear region. This is, of course, good practice anytime, not just for battery operation. Where no GND or V_{CC} is readily available, it's often tempting to connect the unused pin to a well-defined switching pin. However, this isn't recommended with battery-powered systems owing to the redundant circuitry that is then switched.

Use crystal oscillators for low-power consumption

Most oscillators based on logic ICs operate mainly in the linear region so they draw quite significant through-currents. Schmitt-trigger oscillators are the worst offenders in this respect, followed by RC oscillators and then by crystal oscillators.

Power consumption of Schmitt-trigger and RC oscillators is relatively independent of frequency, which means that you derive no advantage from operating them at low frequency, and that their quiescent power consumption is high. Crystal oscillators, on the other hand, have a power consumption that's directly proportional to frequency, so you can operate them at lower frequency to reduce power consumption. For these oscillators, a good choice of operating frequency is 32 kHz because crystals for this frequency are readily available, and the frequency is low enough to give reasonably low power consumption.

Use economical bus structures to save power

In this respect, the non-proprietary CMOS STD Bus (produced by more than eighty manufacturers worldwide) definitely has the edge over the C44 Bus structure. The CMOS STD Bus, developed to match the characteristics of CMOS microprocessors, is a modified and upgraded version of the STD Bus and includes a battery stand-by facility. Major features in its favour are its average current drain and operation time, both of which are about 1/500th that of the C44 Bus.

PRACTICAL CIRCUITS FOR PROVIDING BATTERY BACK-UP

HCMOS ICs, like all other CMOS families, have an input structure that provides excellent protection against ESD. This input structure does, however, mean that you must ensure the supply voltage of the driving system is never more than one diode drop above the driven circuit supply voltage. If it is, current will flow through the input protection diode to V_{CC}, and this will not only cause quiescent power dissipation, it could also damage the diode if it greatly exceeds the diode's maximum d.c. rating I_{IK} (20 mA).

In practice, however, power fed from the normal supply via an output and then via an input protection diode is not totally lost since it does provide power for the battery-powered section. And the diode will be completely safe provided the current to V_{CC} doesn't exceed 20 mA continuously for one input, or 50 mA for several inputs biased simultaneously (if types with bus-driver outputs are used, this latter figure can go as high as 70 mA). What's more, since HCMOS is completely latch-up free, there's no danger of latch-up being caused by any input currents triggering parasitic bipolar structures. If these currents are very large, however, say between 120 and 150 mA, the polysilicon resistors in the diode input circuitry path will burn out.

In the example of Fig.4, HIGH-to-LOW level-shifters 74HC4049 or 74HC4050 are used to prevent the flow of positive input currents into the system due to input voltage levels being greater than one diode drop above V_{CC}. The level shifters simply reduce the input voltages to a level below this value to prevent current flowing through the input protection diode. If the circuit is such that input voltages can still exceed V_{CC} even with level shifters, then external resistors should be included to limit the input currents to 20 mA. External resistors may also be necessary in the output circuits where, if the output voltage can be pulled above V_{CC} or below GND, the currents should be limited to 20 mA. These currents are due to inherent V_{CC}-to-GND diodes that are present at all outputs (including three-state outputs).

To avoid input diode current in the receiving part of Fig.3, the same HIGH-to-LOW level shifters can be used to replace the inverter.

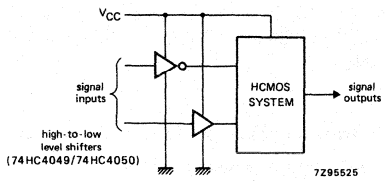


Fig.4 HIGH-to-LOW level-shifters 74HC4049 or 74HC4050 prevent the flow of positive input currents into the system due to input voltage levels being greater than one diode drop above V_{CC}. The level shifters simply reduce the input voltage to a level below this value to prevent current flowing through the input protection diode

Figure 5 shows a very simple circuit for providing battery back-up using a dry battery, or a rechargeable battery if a trickle-charge resistor is used. Diode D_1 is included to ensure that, in normal operation, the main supply voltage never exceeds the voltage of the backed-up supply. If Schottky diodes ($V_f = 0{,}2$ V) are used, however, D_1 can be omitted.

Many designers like to include some kind of regulation circuitry in their battery supply to provide the system with a constant voltage even while the battery voltage decreases during discharge. CMOS circuits, however, can operate directly from batteries despite the voltage decrease with discharge. If, however, the system is designed to run at maximum speed at $V_{CC} = 5$ V and the battery voltage falls to say 3,5 V, a reduced operating frequency will have to be accepted.

Figure 5 provides a power-down failure signal by means of a 74HC04 driven from a higher-voltage (unregulated) supply. If power goes down, the input to the 74HC04 (normally about 5 V) goes to zero, giving an active-LOW shut-down signal.

POWER MANAGEMENT IN BATTERY-POWERED SYSTEMS

Battery backed-up systems should be designed to use very little stand-by power, so your first aim should be to get as good an estimate as possible of the stand-by power P_S in your system. In HCMOS systems, the best estimate of stand-by power can be got by taking all the worst-case I_{CC} quiescent currents for each individual IC and adding them to any termination currents. Table 1 gives you the worst case I_{CC} values for different IC classes of complexity (SSI, FF, MSI).

TABLE 1
Max. quiescent supply current per device category

device complexity	I_{CC} at V_{CC} max 25 °C	85 °C	125 °C
SSI	2 μA	20 μA	40 μA
FF	4 μA	40 μA	80 μA
MSI	8 μA	80 μA	160 μA

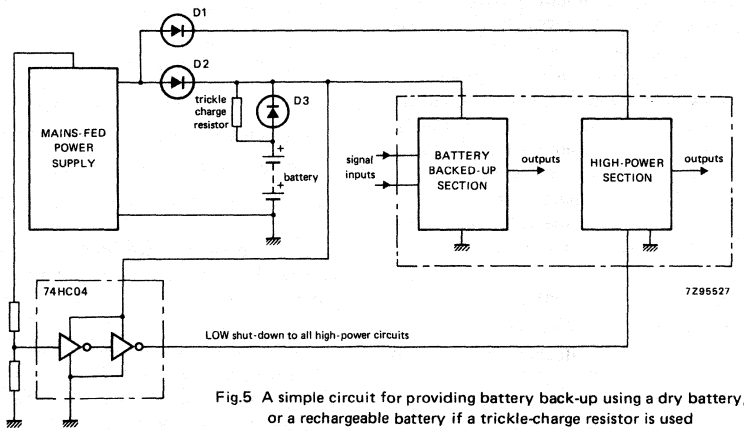


Fig.5 A simple circuit for providing battery back-up using a dry battery, or a rechargeable battery if a trickle-charge resistor is used

The I_{CC} used is determined by the temperature range over which the system will operate. For example, a 74HC00 operating from −40 to +85 °C will have a worst-case I_{CC} of 20 μA.

The total dynamic power dissipation P_D of an HCMOS system was given by expression (1) earlier. The total power P_T of the system will then be the sum of the stand-by power P_S and dynamic power P_D, and the average current delivered by a battery with a voltage V will be:

$$I_{AV} = \frac{\delta P_T}{V}$$

in which δ is the duty factor of the back-up system (estimated power-down time as a fraction of the total operating time). The lifetime of the battery will then be:

$$\text{battery lifetime} = \frac{\text{ampere-hour rating of battery}}{I_{AV}}$$

BATTERIES

Depending on the application, you can provide battery back-up with either rechargeable batteries or dry batteries.

Rechargeable batteries

For applications in which power interruptions may be frequent and of fairly long duration (for example during transport), you should use rechargeable batteries. Here the best choice is still the nickel cadmium battery. This is available in several sizes and can be soldered to a printed circuit board as a discrete component.

Nickel cadmium batteries present very few problem in use, and provided you treat them properly, particularly when charging them, they should have a long and trouble-free life. The best way of keeping them fully charged is to incorporate a trickle-charging circuit that provides a low, continuous current (roughly 0,03 × cell capacity). Expect a nominal operating voltage of 1,25 V per cell, and a minimum voltage of about 1 V per cell.

The alternative to the nickel-cadmium battery: the sealed lead-acid battery has a nominal voltage per cell of of about 2 V and a lower limit of 1,8 V. Like the nickel-cadmium battery it requires no maintenance. It's best used where charging may be infrequent, say after several hours of operation. Its shelf discharge rate is lower than that of a nickel-cadmium battery and when fully charged, it will have a shelf life of about two years.

Dry batteries (non rechargeable)

You can use dry batteries in applications where power interruptions are likely to be seldom and short. Six options are available:

Leclanché batteries possess the following advantages:

- they can be bought almost anywhere
- and they fit into standard fittings

and the following disadvantages:

- their life is relatively short
- their power is relatively low
- they're rather bulky
- and even with intermittent loading, their discharge rate is high.

Their nominal operating voltage is around 1,5 V per cell down to a minimum of around 1 V per cell.

Alkaline batteries posses the same advantages as Leclanché batteries. And they have the additional advantages of being able to provide greater power (especially for loads with heavy and continuous current drain), and of being able to operate at lower temperature (down to −20 °C).

Zinc-Mercury batteries posses the following advantages:

- they're compact
- they have a fairly flat discharge characteristic
- and they provide relatively high power

and the following disadvantages:

- they're not easy to acquire (normally only available from specialist suppliers)
- their life is relatively short
- they're not suitable for delivering high currents
- they don't operate well at low temperature
- and they can't be used in standard fittings.

Their nominal voltage is around 1,35 V per cell.

Zinc-silver batteries have about the same advantages and disadvantages as zinc-mercury batteries and a nominal voltage of 1,5 V.

Zinc-air batteries have the same advantage and disadvantages as zinc-mercury and zinc-silver batteries and like zinc-silver batteries they have a nominal voltage of 1,5 V per cell. They also have an operating life almost double that of the other two types.

TABLE 2
Characteristics of lithium batteries

cathode material	operating voltage (V)	energy density (Wh/kg)	discharge rate	seal type	operating temp. (°C)	size
iodine	2,8	140	low to 0,5 Ah	hermetic	−55 to +125	small
carbon mono-fluoride	2,7	280	medium to 1 Ah	plastic crimp	−20 to +55	large
manganese dioxide	3	270	medium to 1 Ah	plastic crimp	−20 to +55	large
copper oxide	1,7	300	medium to 1 Ah	plastic crimp	−55 to +125	large
sulphur dioxide	2,8	330	1 Ah and more	hermetic vented	−55 to +75	

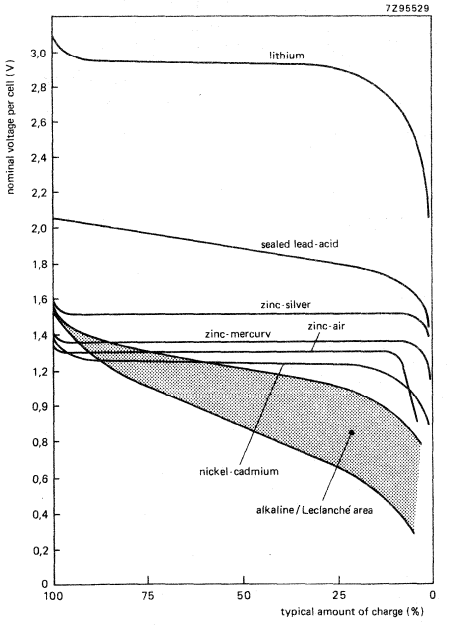


Fig.6 Cell voltage as a function of charge for various batteries

Lithium batteries possess the following advantages:

- they have a high voltage per cell (say a minimum of 2 V)
- they have a long shelf life (greater than 10 years)
- they're compact (often disc-shaped so they can be easily soldered to a print board)
- they have a very flat discharge characteristic (see Fig.6)
- their wide operating temperature range matches perfectly that of HCMOS
- and finally, they offer you the highest energy density of all batteries

and the following disadvantages:

- like mercury batteries they're not always easy to find
- and they can't be used in standard fittings.

So, wherever power interruptions are likely to be seldom and short, your best choice is undoubtedly the lithium battery, the characteristics of which are given in Table 2. The disadvantage of not being able to use it with standard fittings will be of little importance since in normal applications you'll only need to renew the battery once every 10 years so it can be soldered into the circuit.

Finally, to help choose the best battery for your application, we've included Table 3 which shows the major parameters of various types of battery.

TABLE 3
Major specifications of various batteries

	nominal voltage (V)	typical capacity (Ah)	operational power (W/kg)	operational energy density (Wh/kg)	operational energy density (Wh/cm³)	temperature range storage (°C)	temperature range operating (°C)	shelf life to 80% capacity (months)
Dry batteries (non-rechargeable)								
Lechlanché								
– ammonium chloride	1,5	0,05 - 30	1,0	45	0,12	–40 to 50	– 6 to 50	6 - 24
– zinc chloride	1,5	0,1 - 9	1,5	88	0,18	–40 to 70	–17 to 70	30
alkaline	1,5	0,1 - 20	2,0	92	0,22	–40 to 50	–30 to 55	30
zinc-mercury	1,35 - 1,4	0,02 - 28		120	0,39	–40 to 60	0 to 55	30
zinc-silver (monovalent)	1,5	0,04 - 0,3		120	0,48	–40 to 60	0 to 55	18
zinc-air	1,4	0,2 - 0,3		500	1,45	–40 to 60	– 8 to 55	30
lithium	3,0	1,1 - 10		330	0,53	–50 to 70	–40 to 70	60
Rechargeable batteries								**charge cycles**
lead acid (sealed)	2,0	0,03 - 25	3,5	30	0,1	–40 to 60	–40 to 60	100 - 500
nickel-cadmium (sealed)	1,2	0,02 - 5	35	35	0,09	–40 to 60	–20 to 45	300 - 2000

Courtesy of Philips Lighting Division.

PROTECTION OF HCMOS LOGIC ICs IN THE AUTOMOTIVE ENVIRONMENT

With the exception of car radio components, the first electronic components to be used for automotive applications appeared about twenty years ago in voltage regulators. New functions which could be performed by electronic components appeared in the mid-seventies but, unfortunately, these had not been anticipated by electronic component manufacturers who, at that time, had insufficient knowledge of the characteristics of the automotive environment in which their components would have to operate. Today, the situation is much different and electronic components and assemblies are being used, or being developed, for a multitude of automotive functions such as engine management, displays, single-cable switch-units and all manner of accessories.

One thing that hasn't changed is the harsh environment in which electronic components for the automotive industry must work. However, much research has been done to fully characterize the automotive environment so that it is now possible to make real worst-case designs instead of following the rather haphazard approach of twenty years ago. Furthermore, more suitable electronic components such as high-speed CMOS (HCMOS) logic ICs of the 74HC/HCT/HCU family are now available for these applications. Special features that make HCMOS ICs attractive for automotive applications are:

- high noise immunity
- 5 V logic retains speed when battery is almost flat
- input current up to 20 mA d.c. permitted
- low power consumption
- output short-circuit proof
- very low d.c. coupling between adjacent inputs
- latch-up free
- operating temperature range −40 °C to +125 °C
- all types available in 74HCT versions with TTL switching levels
- all types available in DIL or space-saving SO (small outline) packages

This article first discusses the automotive environment, and then outlines logic system design practices for protecting the power supply inputs, and signal inputs/outputs of HCMOS logic ICs against it.

THE AUTOMOTIVE ENVIRONMENT

Extensive studies have been made by electronic component manufacturers and the automotive industry to characterize the climatic and electrical environment which exists in motor vehicles. The results of these studies have been published by the Society of Automotive Engineers (SAE) and the International Standardization Organization (ISO). This information is supplemented by numerous methods of testing electronic components published by most motor-vehicles manufacturers. However, these test methods have many similarities because they are all modelled on the results of the previously mentioned environmental studies. The data on electrical disturbances presented in this article are based on information published by the ISO.

Thermal conditions

From the point of view of temperature, the automotive environment is divided into two main areas; the passenger compartment and the engine compartment. In the passenger compartment of a vehicle in Europe, the temperature can vary from −40 °C on a cold winter morning in Scandinavia to 75 °C on a hot summer afternoon in Spain. In most places in the engine compartment, the temperature will only reach 125 °C (including automatic gearbox, engine block etc.), but care must be taken to avoid mounting electronic assemblies close to very hot items such as exhaust pipes.

The foregoing thermal conditions regularly lead to temperature cycling at a rate of 40 °C/minute and a need for an IC operating temperature range of −40 °C to +85 °C in the passenger compartment, and −40 °C to +125 °C in the engine compartment. The 74HC/HCT/HCU family of HCMOS ICs are specified for both of these temperature ranges and are therefore suitable for use in all automotive applications.

Vibration

In general, the vibration present in the engine compartment of a motor vehicle prohibits the use of ICs in sockets. Even in the passenger compartment, IC sockets should only be used for ICs that have to be interchangeable to suit various applications, for example, PROMs. Remember that all HCMOS ICs also available in SO (small outline) packages which generate lower acceleration forces than ICs in DIL packages because of their significantly lower mass.

Contaminants

The engine compartment of a motor-vehicle is an especially dirty environment due to the presence of salt spray, oil, hydraulic fluid, petrol, dust, sulphuric acid, water and anti-freeze. Special care must therefore be taken when designing housings, connectors, coatings and wiring for electronic equipment to be located in an engine compartment. This subject is adequately covered in many other publications and will not be discussed further here.

Electrical disturbances

During normal running, the voltage available from a 12 V motor-vehicle electrical system will be between 11 V and 16 V. There are, however, some conditions during which the supply voltage will be subject to transient disturbances. The characteristics of many of these disturbances have been specified by the ISO. The ISO test pulses which simulate them should be connected to the system under test via the artificial battery supply network shown in Fig.1.

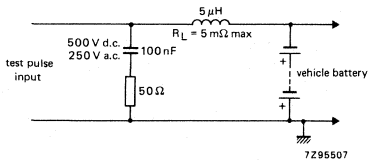


Fig.1 Artificial battery network

Static overvoltage. If a battery is flat after long-distance transport of a new vehicle, it will sometimes be disconnected and an external 24 V battery connected to the system. Electronic equipment must be able to withstand the extra voltage for five minutes if the equipment is connected directly to the battery terminals, or for fifteen seconds if it's connected to the battery via the ignition switch. In some cases, it may also be necessary for electronic equipment to function correctly during these periods.

Static reverse voltage. A battery may be inadvertently reverse connected to a motor-vehicle's electrical system during battery replacement or emergency starting. Electronic equipment must be able to withstand this reverse voltage for at least one minute (all other conditions worst-case). It is not necessary for electronic equipment to function correctly during this period.

Transients due to disconnection of parallel load. If an item of electronic equipment remains connected in parallel with a highly inductive component (e.g. starter motor, solenoid, air-conditioning system, fuel pump, relay or horn) after the latter is disconnected from the battery, the electronic equipment supply input will be subjected to a negative-going voltage transient of up to −100 V. The characteristics of this transient, as published by the ISO, are shown in Fig.2.

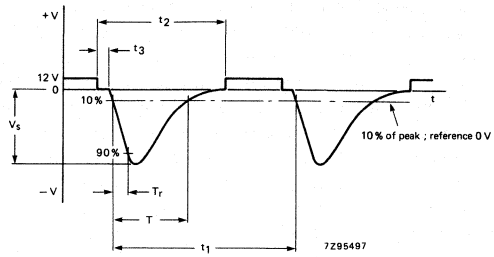


Fig.2 Pulse due to disconnection of an inductive load in parallel with electronic equipment (ISO test pulse 1). V_s = −100 V, R_i = 10 Ω, T = 2 ms, T_r is given in Table 1, t_1 = 0,5 to 5 s, t_2 = 0,2 s, t_3 < 100 μs (the shortest possible time between disconnection of the supply source and application of the pulse)

Transients due to disconnection of series load. If an item of electronic equipment is connected in series with a highly inductive component which is suddenly switched off, the electronic equipment supply input will be subjected to a positive-going voltage transient of up to 100 V. The ISO has published the characteristics of this transient as shown in Fig.3. Electronic equipment must be able to withstand several thousand repetitions of the transient which occur at a repetition rate of between twice per second and twelve times per minute.

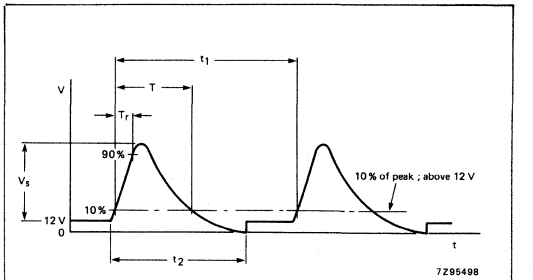


Fig.3 Pulse due to disconnection of an inductive load in series with electronic equipment (ISO test pulse 2). V_s = + 100 V, R_i = 10 Ω, T = 0,05 ms to 0,2 ms, T_r is given in Table 1, t_1 = 0,5 to 5 s, t_2 = 200 ms

Switching spikes. Switching spikes with peak levels up to 100 V can be superimposed on a motor-vehicle's 12 V supply due to the distributed capacitance and inductance of the wiring harness. The characteristics of negative-going and positive-going spikes as published by the ISO are given in Fig.4 and Fig.5 respectively.

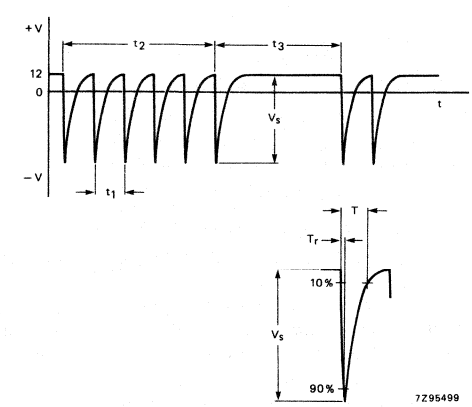


Fig.4 Negative-going switching spikes (ISO test pulse 3a). V_s = −150 V, R_i = 50 Ω, T = 0,1 μs, T_r is given in Table 1, t_1 = 100 μs, t_2 = 10 ms, t_3 = 90 ms

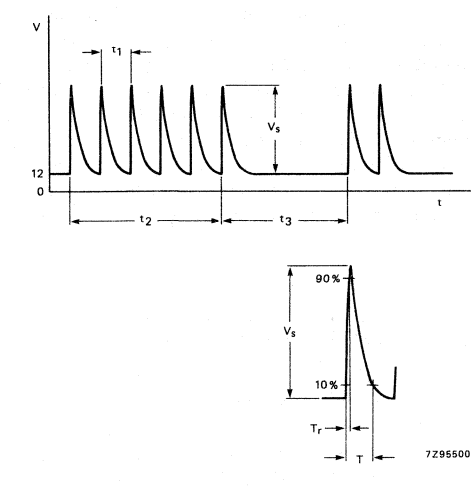


Fig.5 Positive-going switching spikes (ISO test pulse 3b). V_s = +150 V, R_i = 50 Ω, T = 0,1 μs, T_r is given in Table 1, t_1 = 100 μs, t_2 = 10 ms, t_3 = 90 ms

TABLE 1
Rise time as a function of duration for ISO test pulses in Fig.2 to Fig.5

pulse duration (T)	rise time (T_r)
100 ns	6 ns
1 μs	20 ns
10 μs	70 ns
50 μs	150 ns
100 μs	200 ns
200 μs	300 ns
1 ms	800 ns
2 ms	1 μs

Low-voltage noise transients. Transient reductions of the nominal 12 V supply to around 5 V occur during engine starting due to the varying load imposed by the starter motor as it rotates the crankshaft. Since the viscosity of sump oil increases at lower temperatures, the amplitude of these transients increases with decreasing temperature. The ISO test waveform for this condition is given in Fig.6. The test should be repeated several times. All electronic components should remain undamaged by the test and any component associated with engine management must remain operational throughout the test.

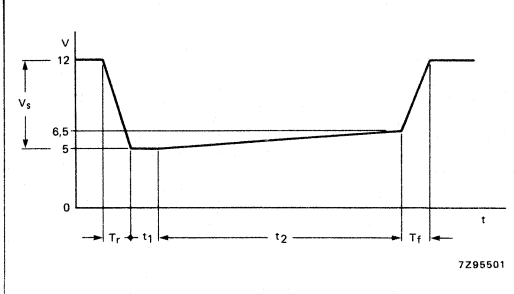


Fig.6 Starter motor engagement interference (ISO test pulse 4) V_s = 7 V, R_i = 0,01 Ω, T = 130 ms, T_r = 10 ms, t_1 = 10 ms, t_2 = 100 ms, T_f = 10 ms

Load dump. A positive-going transient is superimposed on the nominal 12 V supply if a large load or flat battery is disconnected from the electrical system of a vehicle whilst the engine is running at high speed. The peak amplitude of the transient will be between 10 V and 120 V depending on the level of alternator field excitation at the instant the load

or battery is disconnected, and its duration will be between 40 ns and 400 ms depending on the time-constant of the alternator field excitation circuit. This is the most severe transient to which electronic equipment can be subjected in the automotive environment. Although several vehicle manufacturers are currently working on central suppression of load dump transients it must be assumed, for the time being, that there is still a possibility that they will occur. The test pulse specified by the ISO for load dump transients is shown in Fig.7.

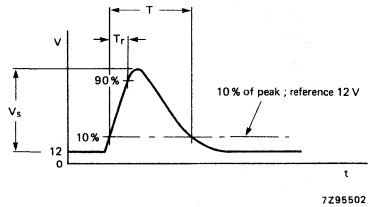


Fig.7 Pulse due to load dump (ISO test pulse 5).
V_s = 10 V to 120 V, R_i = 0,5 to 4 Ω,
T = 40 to 400 ms, T_r = 5 to 10 ms

Transient due to ignition coil interruption. If the ignition coil is interrupted, a negative-going impulse with a peak amplitude of up to −300 V will occur on the electrical system supply line. The test pulse specified by the ISO for this condition is shown in Fig.8.

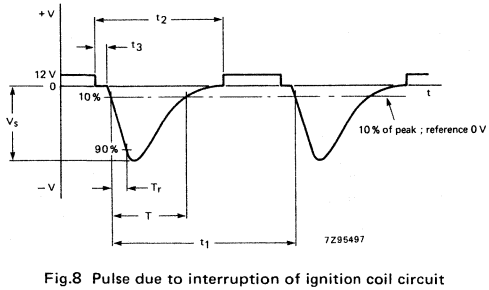


Fig.8 Pulse due to interruption of ignition coil circuit (ISO test pulse 6).
V_s = −300 V, R_i = 30 Ω, T = 300 μs, T_r = 60 μs,
t_1 = 15 s, t_2 = 1 s, t_3 < 100 μs
(the shortest possible time between disconnection of the supply source and application of the pulse)

Transient due to alternator field decay at ignition switch-off. When the ignition of a motor vehicle is switched off, the field windings of the alternator lose their energy and cause a negative-going transient with a peak amplitude of up to −80 V on the electrical system supply line. The test pulse specified by the ISO for this condition is shown in Fig.9.

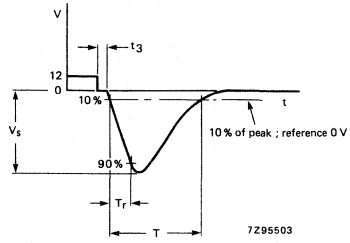


Fig.9 Pulse due to alternator field decay (ISO test pulse 7).
V_s = −80 V, R_i = 10 Ω, T = 100 ms, T_r = 0,5 to 10 ms,
t_3 < 100 μs
(the shortest possible time between disconnection of the supply source and application of the pulse)

Arc-over transient. An arc-over transient occurs if a sparking plug lead or high-tension lead from the ignition coil accidentally falls close to an electronic assembly, or if a spark is intentionally drawn from the h.t. distribution system of a motor-vehicle during servicing. There is no ISO test pulse for this condition but electronic assemblies must be able to withstand h.t. sparks to the case and to all supply and ground connections (not to signal inputs or outputs).

Electrostatic discharge. The terminals of an electronic unit can be subjected to electrostatic discharges during vehicle assembly or during repair or replacement of the unit. Any electronic equipment with driver-operated controls may also be subjected to repeated electrostatic discharge via the driver's body throughout the life of the vehicle. A method commonly used to simulate these electrostatic discharges is to charge a 100 pF capacitor to ±10 kV and then discharge it, via a resistor (560 Ω specified by ISO but the industry standard is 1,5 kΩ) and the pin(s) or lead(s) of the electronic component or assembly under test.

PROTECTING ELECTRONIC SYSTEMS FROM THE AUTOMOTIVE ENVIRONMENT

The power supply line, housing, signal inputs and signal outputs of HCMOS electronic systems for automotive applications must all be protected from the harsh operating environement encountered in all types of motor-vehicles. Although it is not possible to devise a universally-applicable protection scheme, the remainder of this article will be devoted to recommendations for protecting electronic systems which contain high-speed logic ICs of the 74HC/HCT/HCU family.

Type of housing

Because of the risk of arc-over from the h.t. leads, electronic equipment in the engine compartment should be in a metal case connected to the bodywork or chassis of the vehicle. Electronic equipment in the passenger compartment is not exposed to this hazard and can therefore be housed in a case made from any material.

HCMOS IC supply line protection

Electronic equipment supply lines in vehicles must be protected against all the previously discussed electrical disturbances. In addition, they must be able to continue to supply items such as engine management systems and trip computers with sufficient energy to allow them to operate normally during the low voltage noise transients that occur during operation of the starter motor.

The previously discussed ISO requirements are so diverse that the only method of completely meeting them for CMOS logic ICs would be to incorporate on-chip integrated zenering; indeed, this method is commonly used for custom ICs. However, the high power handling requirements would lead to the use of too large an area of silicon to justify the use of this method for standard ranges of logic ICs. Furthermore, many of today's applications use multiple IC technologies in which a multitude of unforeseen interactions can occur. All these factors indicate that the best solution to the problem of operation of electronic systems in the harsh automotive environment is to have a central stepped-down (5 V) stabilized power supply which also incorporates decoupling and noise filtering. However, since vehicle manufacturers have no yet universally accepted this philosophy, additional precautions must be taken to protect the supply units of electronic systems containing HCMOS ICs.

For low current applications (up to 20 mA), the supply line protection circuit given in Fig.10 can be used. The component values which allow continued operation during 10 seconds of starter motor operation are given in Table 2.

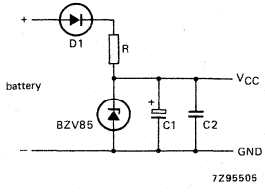


Fig.10 Protection for a low current power supply

TABLE 2
Component values for the circuit of Fig.10

supply current	R	C1
5 mA	560 Ω	60 mF
10 mA	330 Ω	80 mF
20 mA	220 Ω	220 mF

If continued operation during engine starting is not required, D_1 can be omitted (the zener diode also absorbs negative-going transients) and the value of C_1 can be decreased to 22 μF.

If it's necessary to supply more than 20 mA, the use of a zener diode is not recommended because its power dissipation would be too high. It's better to use the arrangement shown in Fig.11 which incorporates one of the voltage regulators specially designed for automotive applications. These regulators have a very low forward voltage drop (0,2 V at 150 mA and 0,4 V at 400 mA) combined with adequate protection against all the electrical disturbances encountered in a motor-vehicle. The low forward voltage drop of the regulator ensures that HCMOS logic ICs will remain operational during starter motor operation without the need to use the extremely high values of electrolytic capacitor (C_1) specified in Table 2 for the circuit in Fig.10.

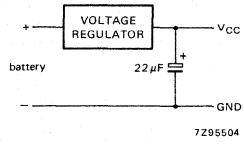


Fig.11 Protection for a higher current power supply

HCMOS IC input protection

Having taken precautions to protect the supply line, it may seem that the ICs are now fully protected against the automotive environment, but there are still two important points that need attention. Firstly, the 2-rail power supply system puts the burden of sequencing on the electronic equipment designer. Secondly, the input device (sensor, actuator) is still in a harsh environment. Taking a simple door contact as an example, the following requirements must be met:

– the contact must pass at least 20 mA to ensure self-cleaning

– since the signal lines are still subject to 150 V transients, additional resistance must be added in series with HCMOS inputs to reduce forward current through the input protection network to a safe level. The graph in Fig.12 shows safe levels of input current as a function of pulse duration

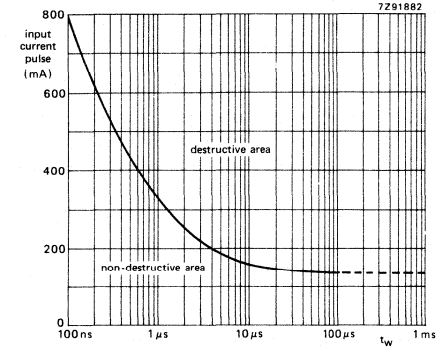


Fig.12 HCMOS input current as a function of pulse duration

– radio-frequency interference from within the vehicle (e.g. ignition) or from external sources such as strong CB transmissions can easily swamp input signals from an input sensor. It is good practice to bypass r.f.i. to ground with a capacitor immediately after the input connector to the electronic equipment

– the point at which a simple mechanical contact makes or breaks is often poorly defined. Debouncing is therefore essential and the resulting signal should also be conditioned by a Schmitt trigger.

The circuitry shown in Fig.13 conforms to the foregoing requirements. Resistor R_1 ensures that at least 20 mA flows through the contact. Capacitor C_1 should have a value of 22 nF to 100 nF to decouple r.f.i. immediately after the electronic equipment connector.

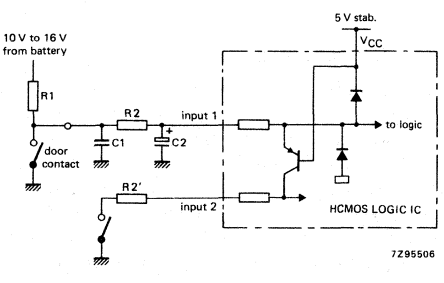


Fig.13 Applying a signal from a simple door contact to an HCMOS IC

In most cases, the input signals from several sensors are received by a single CMOS IC. There is then a possibility of interaction between adjacent inputs via the parasitic bipolar transistor shown in Fig.13. Current injected into the substrate at one input is partially diverted to an adjacent input where it manifests itself as a 'leakage' current. This phenomenon is described in more detail under the heading 'coupling of adjacent inputs' in the User Guide section. If the contact at the adjacent input is closed, the 'leakage' current causes a voltage to be developed across R_2, which may exceed V_{ILmax}. HCMOS ICs have two guaranteed parameters which prevent this from happening:

– the h_{FE} of the parasitic bipolar transistor is 0,05 max.

– the worst-case LOW input level is 30%V_{CC} compared to 20%V_{CC} for standard CMOS logic.

In a 5 V HCMOS-based electronic system in a vehicle, the maximum allowable input current to prevent degradation of a LOW level at an adjacent input is:

$$\frac{V_{IL\,max}}{h_{FE}\,R_2'} = \frac{0{,}3 \times 5}{0{,}05 \times R_2'} = \frac{30}{R_2'} \qquad (1)$$

The current into the input can also be described as:

$$\frac{V_{bat} - V_{CC}}{R_1 + R_2} = \frac{16 - 5}{R_1 + R_2} = \frac{11}{560 + R_2} \qquad (2)$$

Since equations (1) and (2) are equal, and assuming $R_2 = R_2'$:

$$\frac{30}{R_2} = \frac{11}{560 + R_2}$$

which expressed in terms of R_2 gives:

$$R_2 = -\frac{16800}{19} = -884\ \Omega.$$

Since the resulting value of R_2 is negative, the calculation proves that interaction between inputs which causes a problem with conventional 4000 series CMOS logic is no longer a problem with HCMOS logic. The value of R_2 can therefore be chosen solely for limiting the input current to the maximum HCMOS rating. For positive input current into HCMOS inputs, this is 20 mA for one input or 50 mA total for all inputs of a package. For negative current, it is 14 mA for one input, 9 mA for two inputs, 6 mA for three inputs, 5 mA for four inputs, 4 mA for five inputs and 3 mA per input for more than five inputs. Assuming a worst-case pulse amplitude of 150 V and a maximum input current of 10 mA, the value of R_2 would be 15 kΩ. However, a designer might elect to increase this value to obtain the debouncing time-constant in conjunction with C_2 (high value resistors are cheaper than high value capacitors!).

A time-constant of at least 200 ms should be used for simple contacts which are often manufactured to achieve a compromise between mechanical rigidity and price.

HCMOS IC output protection

According to the HCMOS family specification, it's not permissible to short-circuit the output of HCMOS ICs. Nevertheless, this sometimes happens. For example, a breakdown mechanic could inadvertently short a signal line to an injection coil to the bodywork, or an engineer servicing an electronic module could short an output to GND with a probe (printed-circuit boards are very densely packed nowadays). Our development engineers have anticipated this and designed the aluminium tracks to HCMOS outputs to be able to carry short-circuit current. Laboratory experiments have confirmed that HCMOS ICs are indeed short-circuit proof.

A potential hazard for all CMOS ICs is the possibility of latch-up being initiated by excess input/output current or supply overvoltage. This is a real possibility in a motor-vehicle where the ICs are often supplied by the unfiltered voltage from the battery which is usually at least a metre away. Also, the nanosecond rise and fall times of IC signals can be reflected by actuator inputs and, due to voltage-doubling at the end of the cable, travel back and cause overshoots or undershoots at IC outputs. If an IC is driving a power npn transistor, the base pin of which becomes shorted to the collector for some reason, 12 V will be applied directly to the IC output. A resistor must therefore be connected in series with the IC output. Its value must be chosen not only to allow sufficient base drive for the power transistor, but also to limit the output current of the IC to a level that doesn't cause latch-up, even during fault conditions. The latch-up phenomenon has been fully discussed in the article "Standardizing latch-up immunity tests" which explains why, unlike many other CMOS ICs, HCMOS ICs are absolutely latch-up free.

SUITABILITY OF HCMOS ICs FOR MIXED TECHNOLOGY SYSTEMS

The automotive electronics industry selects its components to achieve an optimum balance between price and performance. For example:

- NMOS microprocessors which have LSTTL input/output compatibility are still widely used. All HCMOS ICs are available in 74HCT versions which are TTL-compatible
- many bipolar P(ROMs) which were originally designed in TTL technology are still used for look-up tables etc. 74HCT input levels are compatible with the 0,4 V/2,4 V output swings of these devices
- analog comparators are in widespread use. The output levels from these are the saturation voltages of bipolar transistors (0,4 V or $V_{CC} - 0{,}4$ V). 74HC ICs are ideal for this input voltage swing.

AUTOMATIC ASSEMBLY OF AUTOMOTIVE ELECTRONICS

To aid their drive toward more automated production lines and further miniaturization, manufacturers of electronic equipment for vehicles will appreciate the fact that HCMOS ICs are not only available in DIL plastic packages. All types are also available in SO (small outline) packages; ideal for automated surface mounting.

ASTABLE MULTIVIBRATORS USING HCMOS ICs

74HC/HCT/HCU high-speed CMOS (HCMOS) logic ICs dissipate little power, have a wide operating voltage and temperature range and a low temperature coefficient of the input switching threshold voltage. This makes them ideal for constructing simple yet reliable astable multivibrators in which the operating frequency is determined by a single RC network. What's more, the high impedance of HCMOS inputs allows a wide range of switching time-constants (wide frequency range) to be selected without using high value capacitors which would increase the dynamic power dissipation. This article describes a basic astable circuit using two 74HC/HCU or two 74HCT inverting gates or buffers and derives simple formulae for accurately determining its operating frequency. It then develops the formulae to show how adding one resistor to the circuit makes the operating frequency and duty factor more independent of supply voltage variations and input switching threshold voltage spreads, and limits the input current. The article concludes by discussing the effect of temperature variations, the dynamic power dissipation and the range of external component values and supply voltage that can be used for the circuit.

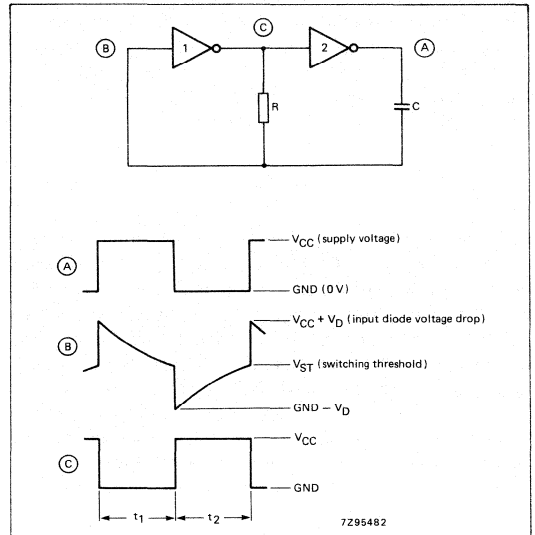


Fig.1 Basic astable multivibrator

BASIC ASTABLE MULTIVIBRATORS

Figure 1 illustrates the circuit arrangement and waveforms for a basic astable multivibrator using two HCMOS inverters. When the supply voltage (V_{CC}) is applied to the circuit, the potential at points A and B will be of opposite polarity to that at point C (e.g. points A and B LOW, point C HIGH). The capacitor then begins to charge and the potential at point B approaches the switching threshold voltage (V_{ST}) of inverter 1. When the voltage at point B reaches V_{ST}, the output of inverter 1 (point C) goes LOW, and the output of inverter 2 (point A) goes HIGH. Because of the level change at point A is rapid, it is transferred to point B. However, point B is clamped within the limits $V_{CC} + V_D$ and GND – V_D by the input protection network of inverter 1. The potential at point B now approaches V_{ST} again and, when it reaches that level, the circuit again changes state and the cycle repeats. The equations for switching periods t_1 and t_2 are:

$$t_1 = -RC \ln \frac{V_{ST}}{V_{CC} + V_D} \quad (1)$$

$$t_2 = -RC \ln \frac{V_{CC} - V_{ST}}{V_{CC} + V_D} \quad (2)$$

$$t_1 + t_2 = -RC \ln \frac{V_{ST}(V_{CC} - V_{ST})}{(V_{CC} + V_D)^2} \quad (3)$$

Influence of supply and switching threshold voltage variation

For a circuit using a 74HC/HCU IC with $V_{ST} = 0{,}5\ V_{CC}$ and $V_D = 0{,}7$ V, the switching period varies by +9% and –2,5% around the value at $V_{CC} = 5$ V over the supply voltage range 3 V to 6 V. This variation is due to the influence of the forward voltage drop across the input protection diodes of inverter 1 ($V_D = 0{,}7$ V) which causes the value

$$\ln \frac{V_{ST}}{V_{CC} + V_D}$$

to vary with supply voltage variations even though V_{ST} is a constant percentage of V_{CC}. Since $V_{ST\,nom.}$ is $0{,}5\ V_{CC}$ for 74HC and 74HCU ICs, the peaks of the voltage at point B in Fig.1 are symmetrical around V_{ST}, resulting in a duty factor of 0,5 which is independent of supply voltage variations. However, the nominal switching threshold voltage is subject to a spread ($0{,}3\ V_{CC}$ to $0{,}7\ V_{CC}$ for 74HC ICs and $0{,}2\ V_{CC}$ to $0{,}8\ V_{CC}$ for 74HCU ICs). This causes the total switching period to increase by a maximum of 10,5% for a circuit using a 74HC IC and 27% for a circuit using a 74HCU IC. The switching threshold voltage spread also causes the duty factor to spread between the limits 0,7 to 0,3 for a circuit using a 74HC IC, and 0,8 to 0,2 for a circuit using a 74HCU IC.

For a circuit using a 74HCT IC, the nominal V_{ST} is 1,3 V at V_{CC} = 4,5 V, 1,415 V at V_{CC} = 5 V and 1,53 V at V_{CC} = 5,5 V. The switching threshold voltage is therefore always below the midpoint of the total voltage swing at point B in Fig.1, and is not a constant percentage of the supply voltage. Because the supply voltage range for 74HCT ICs is only 4,5 V to 5,5 V, the value

$$\ln \frac{V_{ST}}{V_{CC} + V_D}$$

varies less over the supply voltage range than it does for a circuit using a 74HC/HCU IC, resulting in a switching period variation of ±0,8% around the value at V_{CC} = 5 V over the supply voltage range. However, because the voltage swing at point B in Fig.1 is asymmetrical around V_{ST}, the periods calculated with equations (1) and (2) are unequal, resulting in duty factors of 0,74 at V_{CC} = 4,5 V, 0,75 at V_{CC} = 5 V and 0,76 at V_{CC} = 5,5 V. Furthermore, the nominal V_{ST} of 74HCT ICs is subject to a spread of about ±0,5 V. With a 5 V supply, this causes a maximum switching period increase of 16% above the nominal value, and a duty factor spread from 0,8 to 0,6.

CIRCUIT MODIFICATION TO REDUCE SWITCHING PARAMETER VARIATIONS

Figure 2 shows the astable multivibrator circuit modified by the addition of resistor R_S in series with the input to inverter 1. This resistor increases the resistance between point B and the input to inverter 1, and thereby prolongs the discharge of capacitor C via the input protection network of inverter 1 each time the polarity of the charge on capacitor C reverses. If the value of R_S is high enough, the voltage at point B will reach the limits $V_{CC} + V_{ST}$ and $V_{ST} - V_{CC}$ before the voltage at point D reaches the switching threshold voltage. Since the waveform at point B now swings by $\pm V_{CC}$ around V_{ST}, it is always symmetrical about V_{ST} regardless of the value of V_{ST} or V_{CC}. If the value of R_S is too low, the peaks of the waveform at point B will be clipped; if it is too high and a buffered 74HC IC is being used, spurious oscillations or glitches may occur due to stray capacitance C_{t1} causing phase-shifted feedback around inverter 1. It is therefore preferable to use the unbuffered Hex Inverter 74HCU04 for this circuit. The optimum value for R_S is 2R. It will be shown later that increasing the value of R_S beyond 2R doesn't result in any further improvement of the performance of the circuit. The waveform at the input to inverter 1 (point D) is clamped by the input protection diodes to $V_{CC} + V_D$ for positive-going swings, and to $-V_D$ for negative-going swings, but resistor R_S limts the current flow through the input protection network during these periods. The presence of R_S therefore also reduces crosstalk to other inverters in the same package.

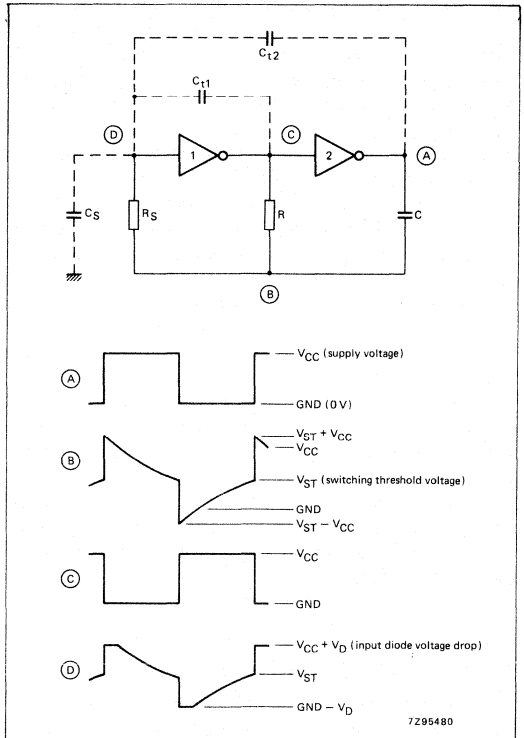


Fig.2 Modified astable multivibrator

Figure 3 is a more detailed version of the waveform at point B in Fig.2. Period t_1 is still defined by equation (1), and period t_2 is still defined by equation (2). The equations for additional periods t_a and t_b are:

$$t_a = -\frac{K}{K+1} RC \ln \frac{K(V_{CC} + V_D)}{K(V_{CC} + V_{ST}) + V_{ST} - V_D} \quad (4)$$

$$t_b = -\frac{K}{K+1} RC \ln \frac{K(V_{CC} + V_D)}{K(2V_{CC} - V_{ST}) + V_{CC} - V_{ST} - V_D} \quad (5)$$

where $K = (R_S + R_I)/R$, and R_I is the input resistance of inverter 1 when one of the input protection diodes is conducting (about 125 Ω).

Since periods t_a and t_b increase with increasing supply voltage, and periods t_1 and t_2 decrease, the total switching period and duty factor of the waveform at point B in the modified circuit tends to be stabilized against supply voltage variations. Since t_a and t_2 increase with increasing switching threshold voltage, and t_1 and t_b decrease, the total

switching period and duty factor also tend to be stabilized against spread of the switching threshold voltage.

If $K \geqslant 2$, periods $t_1 + t_a$ and $t_2 + t_b$ are:

$$t_1 + t_a = -RC \ln \frac{V_{ST}}{V_{CC} + V_{ST}}$$

$$t_2 + t_b = -RC \ln \frac{V_{CC} - V_{ST}}{2V_{CC} - V_{ST}}$$

The total switching period is therefore:

$$T = -RC \ln \frac{V_{ST}(V_{CC} - V_{ST})}{(V_{CC} + V_{ST})(2V_{CC} - V_{ST})} \quad (6)$$

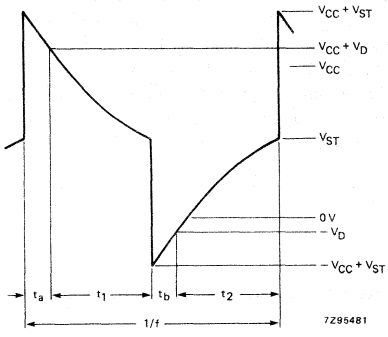


Fig.3 Waveform at point B in Fig.2

Equation (6) shows that the switching period is no longer influenced by the forward voltage drops across the input protection diodes of inverter 1. For a circuit using a 74HC or 74HCU IC in which the nominal value of V_{ST} is $0{,}5V_{CC}$ for all supply voltages, equation (6) can be simplified to:

$$T = 2{,}2RC \quad (7)$$

For a circuit using a 74HCT IC in which the nominal V_{ST} is 1,3 V for $V_{CC} = 4{,}5$ V, 1,415 V for $V_{CC} = 5$ V and 1,53 V for $V_{CC} = 5{,}5$ V, equation (6) can be approximated by:

$$T = 2{,}4RC \quad (8)$$

Tables 1 and 2 verify the accuracy of equations (7) and (8) by comparing their results with calculations made with equations (1), (2), (4) and (5), and with measured results for a circuit in which $V_{CC} = 5$ V and $K = 2$ ($R_S = 2R$).

For a circuit using a 74HC IC, Fig.4 indicates the ratio of measured switching periods to those calculated with equations (1), (2), (4) and (5) for various combinations of R and C and with $K = 2$. The component value limits which will maintain the ratio acceptably close to unity are also shown.

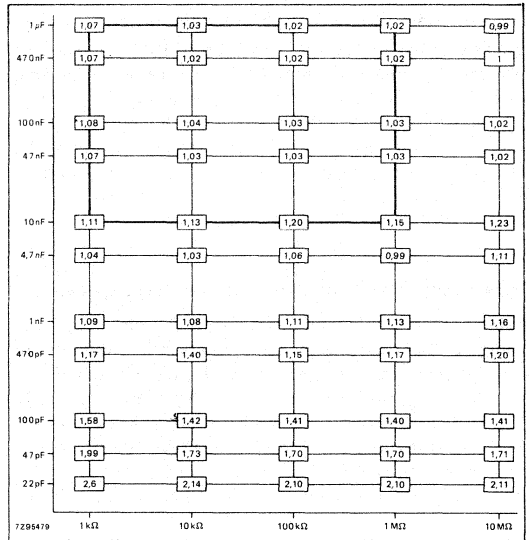


Fig.4 Ratios of measured to calculated switching periods, for a circuit using a 75HC IC, to indicate the validity of equations (1), (2), (4) and (5)

TABLE 1
Accuracy of formulae for 74 HC/HCU ICs with $V_{CC} = 5$ V, $V_{ST} = 2{,}5$ V and $K = 2$ (all times in µs)

RC	T calculated from formulae	T = 2,2 RC	measured T (74HC)	74HCU
1000	2174	2200	2177	2147
100	217	220	218	214
10	21,7	22	22,6	21,7
1	2,17	2,2	2,4	2,4
0,1	0,217	0,22	0,3	0,3

TABLE 2
Accuracy of formulae for 74HCT ICs with $V_{CC} = 5$ V, $V_{ST} = 1{,}415$ V and $K = 2$ (all times in µs)

RC	T calculated from formulae	T = 2,4 RC	measured T
1000	2348	2400	2362
100	235	240	236
10	23,5	24	24,4
1	2,35	2,4	2,6
0,1	0,235	0,24	0,3

Influence of supply voltage variations

Table 3 (74HC/HCU) and Table 4 (74HCT) compare the results of switching period and duty factor calculations made with equations (1), (2), (4) and (5) for $K = 10^{-3}$ (R_S short-circuit), $K = 2$ ($R_S = 2R$) and $K = 10$ ($R_S = 10R$), with supply voltage as a parameter. The Tables show that the influence of supply voltage variation on the switching period and duty factor of a circuit using a 7HC/HCU or 74HCT IC is almost eliminated when $K = 2$.

Influence of switching threshold voltage spread

Table 5 (74HC), Table 6 (74HCU) and Table 7 (74HCT) compare the results of switching period and duty factor calculations made with equations (1), (2), (4) and (5) for $K = 10^{-3}$ (R_S short-circuit), $K = 2$ ($R_S = 2R$) and $K = 10$ ($R_S = 10R$), with switching threshold voltage as a parameter. For a circuit using a 74HC IC, Table 5 shows that the influence of the switching threshold voltage spread on the switching period is reduced by 33% when $K = 2$, and the duty factor spread is reduced by 43%. For a circuit using a 74 HCU IC, Table 6 shows a 33% reduction of the switching period deviation and a 40% reduction of duty factor spread with $K = 2$. For a circuit using a 74HCT IC, Table 7 shows a 29% reduction of switching period deviation and a 25% reduction of duty factor spread when $K = 2$.

Influence of temperature on the switching period

Temperature variations have little influence on the switching period, and hence the operating frequency of astable multivibrators using 74HCMOS ICs. This is because the switching threshold voltage varies by only ±60 mV from its nominal value at 25 °C over the temperature range −40 °C to +125 °C. This is far less than the ±200 mV variation for LSTTL ICs. The effect of the variation of the switching threshold voltage is a spread of the total switching period. For a circuit using a 74HC/HCU IC with a 5 V supply and $K = 2$, the switching period increases by 0,02% at the two temperature extremes. For a circuit using a 74HCT IC, the switching period varies by ±1%.

TABLE 3
Switching period and duty factor as functions of supply voltage with K as a parameter for 74HC/HCU ICs ($V_{ST} = 0{,}5\ V_{CC}$, RC = 100 µs)

	$K = 10^{-3}$				
V_{CC}	3 V	4,5 V	5 V	5,5 V	6 V
total switching period (µs)	181,645	168,685	165,986	163,749	161,866
deviation from value at 5 V	+9%	+1,6%	0	−1,3%	−2,5%
switching duty factor	0,5	0,5	0,5	0,5	0,5

	$K = 2$				
V_{CC}	3 V	4,5 V	5 V	5,5 V	6 V
total switching period (µs)	218,027	216,822	216,537	216,293	216,081
deviation from value at 5 V	+0,7%	+0,0,1%	0	−0,1%	−0,2%
switching duty factor	0,5	0,5	0,5	0,5	0,5

	$K = 10$				
V_{CC}	3 V	4,5 V	5 V	5,5 V	6 V
total switching period (µs)	219,367	219,107	219,045	218,991	218,945
deviation from value at 5 V	+0,1%	+0,03%	0	−0,02%	−0,05%
switching duty factor	0,5	0,5	0,5	0,5	0,5

TABLE 4
Switching period and duty factor as functions of supply voltage with K as a parameter for 74HCT ICs (R_C = 100 μs)

	K = 10^{-3}		
V_{CC}	4,5 V	5 V	5,5 V
V_{ST}	1,3 V	1,415 V	1,53V
total switching period (μs)	188,273	186,810	185,623
deviation from value at V_{CC} = 5 V	+0,8%	0	−0,6%
switching duty factor	0,74	0,75	0,76

	K = 2		
V_{CC}	4,5 V	5 V	5,5 V
V_{ST}	1,3 V	1,415 V	1,53V
total switching period (μs)	234,022	234,855	235,562
deviation from value at V_{CC} = 5 V	−0,3%	0	+0,3%
switching duty factor	0,64	0,64	0,65

	K = 10		
V_{CC}	4,5V	5 V	5,5 V
V_{ST}	1,3 V	1,415 V	1,53 V
total switching period (μs)	236,635	237,692	238,588
deviation from value at V_{CC} = 5 V	−0,4%	0	+0,4%
switching duty factor	0,63	0,64	0,64

TABLE 5
Switching period and duty factor as functions of switching threshold voltage with K as a parameter for 74HC ICs (V_{CC} = 5 V, R_C = 100 μs)

	K = 10^{-3}		
V_{ST}	1,5 V	2,5 V	3,5 V
total switching period (μs)	183,384	165,986	183,384
deviation from value at V_{ST} nom.	+10,5%	0	+10,5%
switching duty factor	0,73	0,5	0,27

	K = 2		
V_{ST}	1,5 V	2,5 V	3,5 V
total switching period (μs)	231,812	216,537	231,812
deviation from value at V_{ST} nom.	+7%	0	+7%
switching duty factor	0,63	0,5	0,37

	K = 10		
V_{ST}	1,5 V	2,5 V	3,5 V
total switching period (μs)	234,596	219,045	234,596
deviation from value at V_{ST} nom.	+7%	0	+7%
switching duty factor	0,62	0,5	0,37

Dynamic power dissipation

The average dynamic power dissipation of an entire IC package of inverters (or inverting gates), only two of which are used for an astable multivibrator is the sum of the following five terms. The first two terms apply to the inverters in the package which don't form part of the multivibrator. The sum of the last three terms is the dynamic power dissipation of the two inverters of the multivibrator.

$C_{PD}V_{CC}^2 f_i$ in which C_{PD} is the load imposed by internal capacitance and switching transient currents, and f_i is the frequency at the input.

$\Sigma(C_L V_{CC}^2 f_o)$ in which C_L is the load capacitance at the output, and f_o is the frequency at the output.

$(C_{PD}V_{CC}^2)/T$ in which C_{PD} is defined for the first term, and T is the total switching period for the multivibrator.

$(2CV_{CC}^2)/T$ in which C is the timing capacitance of the multivibrator, and T is its total switching period.

XV_{CC} in which X is the average through-current from Table 8 and 9. This through current depends on the size of the input transistors of the particular IC and varies from one type of IC to another.

It is obvious from the fourth term that the dynamic power dissipation can be reduced by using a lower value for timing capacitor C, and therefore, higher values for R and R_S.

TABLE 6
Switching period and duty factor as functions of switching threshold voltage with K as a parameter for 74HCU ICs (V_{CC} = 5 V, RC = 100 μs)

	K = 10^{-3}		
V_{ST}	1 V	2,5 V	4 V
total switching period (μs)	210,497	165,986	210,497
deviation from value at V_{ST} nom.	+27%	0	+27%
switching duty factor	0,83	0,5	0,17
	K = 2		
V_{ST}	1 V	2,5 V	4 V
total switching period (μs)	256,202	216,537	256,202
deviation from value at V_{ST} nom.	+18%	0	+18%
switching duty factor	0,7	0,5	0,3
	K = 10		
V_{ST}	1 V	2,5 V	4 V
total switching period (μs)	259,377	219,045	259,377
deviation from value at V_{ST} nom.	+18%	0	+18%
switching duty factor	0,7	0,5	0,3

TABLE 7
Switching period and duty factor as functions of switching threshold voltage with K as a parameter for 74HCT ICs (V_{CC} = 5 V, RC = 100 μs)

	K = 10^{-3}		
V_{ST}	0,93 V	1,415 V	1,9 V
total switching period (μs)	215,996	186,810	171,907
deviation from value at V_{ST} nom.	+16%	0	−8%
switching duty factor	0,84	0,75	0,64
	K = 2		
V_{ST}	0,93 V	1,415 V	1,9 V
total switching period (μs)	261,231	234,856	221,700
deviation from value at V_{ST} nom.	+11%	0	−5,6%
switching duty factor	0,71	0,64	0,58
	K = 10		
V_{ST}	0,93V	1,415 V	1,9 V
total switching period (μs)	264,478	237,692	224,303
deviation from value at V_{ST} nom.	+11%	0	−5,6%
switching duty factor	0,70	0,63	0,57

TABLE 8
Average through-current for two inverters in an astable multivibrator using 74HC/HCU ICs

	74HC00	74HC04	74HCU04
V_{CC}	through-current (μA)		
3 V	150	130	600
4,5 V	700	450	2600
5 V	1050	650	3500
6 V	1800	1050	5600

TABLE 9
Average through-current for two inverters in an astable multivibrator using 74HCT ICs

	74HCT00	74HCT04
V_{CC}	through current (μA)	
4,5 V	700	450
5 V	1050	650
5,5 V	1350	800

The last term is the additional average dynamic power dissipation of the first inverter used for the multivibrator. It occurs because the near-triangular waveform at the input to inverter 1 (point D in Fig.2) slowly approaches V_{ST} and causes the through-current indicated in Tables 8 and 9. Because of the shape of the waveform, inverter 1 is always operating in its linear region so that this term is independent of the operating frequency.

Component value and supply voltage limits

The astable multivibrator shown in Fig.2 will operate correctly as long as C is a bipolar capacitor with a value greater than 100 pF, and the value of R is between 470 Ω and 1 MΩ. The lower limit for the value of R ensure that R is much higher than the output impedance of the inverters (typically 40 Ω with a 4,5 V supply) so that output impedance spreads don't influence the switching period. However, due to the influence of parasitic capacitances C_{t1} and C_{t2}, equations (7) and (8) will only remain valid when C is 10 nF or greater, and R is between 1 kΩ and 1 MΩ.

The previously mentioned spurious oscillations or glitches which can occur if the value of R_S is too large will have a frequency of $1/(2t_p)$ where t_p is the propagation delay of inverter 1. The impedance at the input to inverter 1 is then very high and sensitive to crosstalk. The spurious oscillations can be suppressed by using careful board layout to decrease parasitic capacitance C_{t1}, decreasing R_S, or increasing C_{t2} by connecting a low-value capacitor between point A and D. However, the best solution is to use the unbuffered Hex Inverter 74HCU04 which is specially made for linear applications and will make the oscillator less sensitive to spurious oscillations because it has lower gain than the HC04 or HCT04. Parasitic capacitance C_S is formed by board tracks and should be kept as low as possible to avoid any additional delay due to time-constant R_SC_S.

Although 74HC/HCU ICs can operate from a supply voltage as low as 2 V, it is recommended that a supply of at least 3 V be used for an astable multivibrator. This is because the threshold voltages of the input transistors can be as high as 0,9 V which would leave insufficient margin to operate in the linear region with a 2 V supply. The supply voltage range for astable circuits using 74HC/HCU ICs is therefore 3 V to 6 V. For circuits using a 74HCT ICs it is 4,5 V to 5,5 V.

CRYSTAL OSCILLATORS USING HCMOS ICs

Crystal-controlled oscillators are widely used in clock pulse generators because of their excellent frequency stability and their wide operating frequency range. If they use an HCMOS IC as the active element, they have the additional advantages of low power dissipation and stable operation over a wide range of supply voltages and temperature. This article describes the design of several types of crystal-controlled oscillators based on the unbuffered HCMOS Hex Inverter 74HCU04.

The terms and definitions for crystal-controlled oscillators as specified by the IEC in their publication IEC 122-11 are listed in Table 1.

CRYSTAL CHARACTERISTICS

Figure 1 is the equivalent circuit of a quartz crystal. The reactive and resistive components of the impedance of the crystal alone, and of the crystal with a series and a parallel capacitive load are shown in Fig.2.

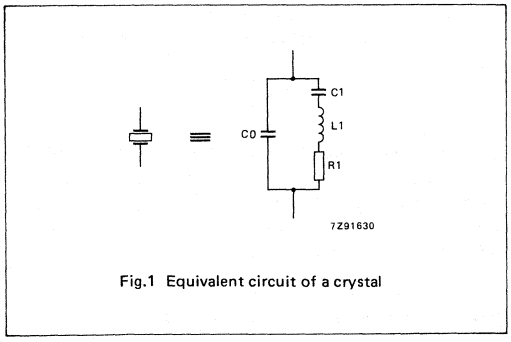


Fig.1 Equivalent circuit of a crystal

Figure 2 shows that, with a specified value of load capacitance (C_L), the load resonance frequency (f_L) is the same for a circuit with either a parallel or series capacitive load. It is therefore very important to use this value of load capacitance in the design of a crystal oscillator. However, the preferred load capacitance should be partially adjustable so that compensation can be made for spurious capacitances caused by the pcb and the pins of the IC. Preferred values of load capacitance specified for fundamental frequency operation of various crystals at parallel resonance are 20 pF, 30 pF, 50 pF and 100 pF. Some countries still use 32 pF, but, since this is not a preferred value, its use is not recommended. The preferred values of load capacitance for overtone operation at series resonance are 8 pF, 12 pF, 15 pF, 20 pF and 30 pF.

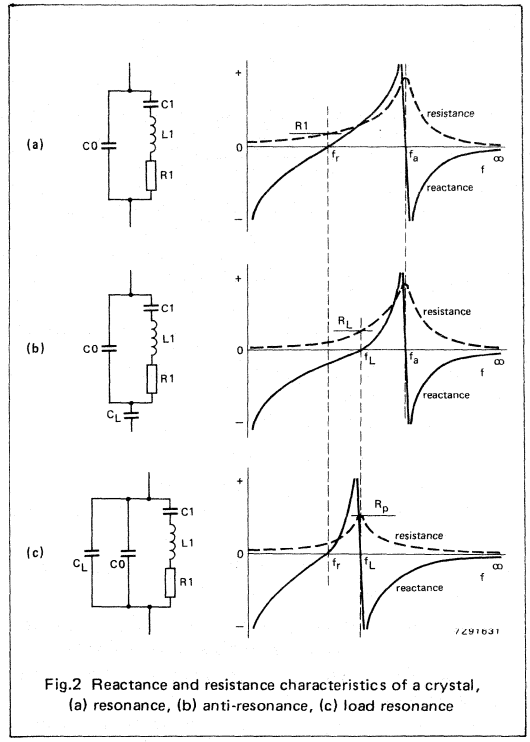


Fig.2 Reactance and resistance characteristics of a crystal, (a) resonance, (b) anti-resonance, (c) load resonance

The power dissipated in a crystal is called the "level of drive". Since the crystal characteristics become highly dependent on the level of drive if it is outside the range 1 pW to 1 mW, the crystal characteristics are usually specified at 0,5 mW. With a very low level of drive, as can occur during oscillator start-up, the characteristics can vary slightly, in particular, the resonance resistance R_r will increase about threefold. To overcome this, the loop gain of the oscillator circuit should be sufficient to prevent start-up problems, but not enough to overdrive the crystal.

HCMOS HEX INVERTER 74HCU04 IN CRYSTAL-CONTROLLED OSCILLATORS

The Pierce oscillator in which the crystal has a parallel load capacitance is the type most widely used in digital systems.

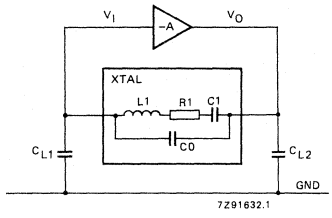


Fig.3 Basic Pierce oscillator

As shown in Fig.3, it is basically a Colpitts oscillator in which the inductor has been replaced by a crystal. The advantages of this configuration are:

- good suppression of the third overtone (9x)
- lower power dissipation (level of drive) in the crystal than in a series-resonant oscillator due to the high ohmic loading
- the amplifier must provide 180° phase shift, so a simple inverter can be used.

The high input impedance of the 74HCU04 Hex Inverter makes it ideal for use in a Pierce oscillator. However, good power supply decoupling is necessary (see section "Power supply decoupling").

Although the 74HCU04 can operate from a supply voltage as low as 2 V, it is recommended that a supply of at least 3 V be used for a crystal-controlled oscillator. This is because the threshold voltages of the input transistors can be as high as 0,9 V which would leave insufficient margin to operate in the linear region with a 2 V supply. The supply voltage range for crystal oscillators using the 74HCU04 is therefore 3 V to 6 V.

Unfortunately, the output impedance of the 74HCU04 is too low to drive the crystal directly. The simple expedient of adding a resistor in series with the output causes additional phase shift resulting in an increase of loop gain and a decrease of the level of drive in proportion to the square of the frequency. This arrangement is therefore only suitable for lower frequencies (up to about 4 MHz). For higher frequency oscillators, the output impedance of the inverter must be increased with a series capacitor instead of a series resistor.

A 4 MHz crystal oscillator using the 74HCU04

Figure 4 illustrates a practical 4 MHz Pierce oscillator in which the crystal is operating at its fundamental frequency and is tuned by a parallel load capacitance consisting of C_{L1} and C_{L2} in series, together with stray capacitances.

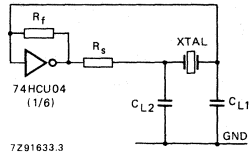


Fig.4 Practical Pierce oscillator using unbuffered inverter 74HCU04

C_{L1} should be adjustable so that the capacitive load can be accurately set to the preferred load capacitance specified for the particular crystal being used. The loop gain of the circuit is:

$$\frac{V_O}{V_I} = \frac{C_{L2}}{C_{L1}}$$

For an economy range 4 MHz crystal (4322 143/144 04091), the specified C_L (C_{L1} and C_{L2} in series) is 30 pF and the specified resonance resistance (R_r) of the crystal is 75 Ω. At 4 MHz, a loop gain (C_{L2}/C_{L1}) of about unity is adequate, and so if there is no stray capacitance.

$$C_{L1} = C_{L2} = 60\ pF.$$

However, since there will always be some stray capacitance 56 pF capacitors should be used for C_{L1} and C_{L2}. Since C_{L1} and C_{L2} are equal, the total impedance as seen from the output of the inverter can be simplified to:

$$Z_L = \frac{X_{CL}^2}{R_r}$$

where $X_{CL} = -j/\omega C_{L2}$ and R_r is the specified resonance resistance of the crystal (75 Ω).

For optimal operation of a Pierce oscillator, the output impedance of the inverter should be the same as the total load impedance. The output impedance of the inverter should therefore be 5,9 kΩ. Since the output impedance of the 74HCU04 with a 5 V supply is only about 40 Ω, the preferred value for R_s in series with the output of the inverter is 5,6 kΩ. However, this value would cause too much phase shift, so a compromise value of 2,2 kΩ is used. Any value between 1 MΩ and 10 MΩ is suitable for R_f which provides d.c. bias for the output of the inverter.

Higher frequency crystal oscillators using the 74HCU04

In addition to the phase shift introduced by R_S in series with the inverter output, the inverter's propagation delay (t_p) also causes phase shift which can be expressed as:

$$\text{Phase shift} = f_{osc} \times t_p \times 360^\circ.$$

With a maximum propagation delay of 14 ns, a 4,5 V supply for the 74HCU04, and an oscillator frequencyof 6 MHz, a further 30° phase shift would occur. This means that the Pierce oscillator circuit shown in Fig.4 is unsuitable for operation at high frequencies. Modifying the circuit by replacing R_S with a capacitor (C_S) of about the same value as C_L (half the value of C_{L1} or C_{L2}), allows the circuit to be used at a higher frequency.

An overtone crystal oscillator using the 74HCU04

Most crystal manufacturers supply crystals for operation at fundamental frequencies, third overtone crystals for operation in the frequency range 10 MHz to 75 MHz, and fifth overtone crystals for operation in the frequency range 50 MHz to 125 MHz.

Due to the high maximum operating frequency of HCMOS logic systems, it may be necessary to use a third overtone oscillator with parallel load capacitance as shown in Fig.5. A critical requirement for this type of oscillator is suppression of the fundamental frequency of the crystal. Two methods of suppression are used in the circuit of Fig.5.

- capacitor C_S, which should have a value close to that of C_L, presents a higher impedance to the fundamental frequency of the crystal than it does to the third overtone
- C_S/L resonates at slightly below the third overtone and traps the fundamental frequency.

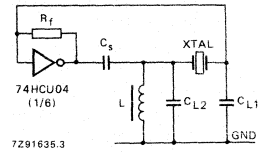


Fig.5 Practical overtone oscillator using unbuffered inverter 74HCU04

Tuning L for maximum output voltage may affect the oscillator frequency slightly, but adjustment of C_{L1} will usually compensate for this.

Checking a prototype crystal oscillator design

The following simple checks will verify the quality of the design of a crystal-controlled oscillator using a 74HCU04 IC:

1. Test the oscillator under worst-case conditions (lowest supply voltage, worst-case crystal and highest operating temperature). A worst-case crystal can be simulated by adding series and parallel resistors.
2. Ensure that the circuit doesn't oscillate without the crystal.
3. Check the frequency stability of the oscillator over a supply voltage range greater than that which is likely to occur during normal operation.

TERMS AND DEFINITIONS FOR CRYSTAL OSCILLATORS (IN ACCORDANCE WITH IEC 122-1)

Adjustment tolerance
The permissible deviation from the nominal frequency at the reference temperature under specified conditions.

Ageing (long-term parameter variation)
The relation which exists between any parameter (e.g. resonance frequency) and time.
Note: such parameter variation is due to long-term changes in the crystal unit and is usually expressed in fractional parts per period of time.

Ageing tolerance
The permissible deviation due to time under specified conditions.

Anti-resonance frequency f_s
The higher of the two frequencies of a crystal unit alone, under specified conditions, at which the electrical impedance of the crystal unit is resistive.

Level of drive
A measure of the conditions imposed upon the crystal unit expressed in terms of power dissipated.
Note: in special cases, the level of drive may be specified in terms of crystal current or voltage.

Load capacitance C_L
The effective external capacitance associated with the crystal unit which ddetermine the load resonance frequency f_L.

Load resonance frequency f_L
One of the two frequencies of a crystal unit in association with a series or with a parallel load capacitance, under specified conditions, at which the electrical impedance of the combination is resistive. This frequency is the lower of the two frequencies when the load capacitance is in series and the higher when it is in parallel (see Fig.2). For a given value of load capacitance (C_L), these frequencies are identical for all practical purposes and are given by:

$$\frac{1}{f_L} = 2\pi \sqrt{\frac{L_1 C_1 (C_0 + C_L)}{C_1 + C_0 + C_L}}$$

Load resonance resistance R_L
The resistance of the crystal unit in series with a stated external capacitance at the load resonance frequency f_L.
Note: the value of R_L is related to the value of R_r by the following expression:

$$R_L = R_r \left(1 + \frac{C_0}{C_L}\right)^2$$

Motional capacitance C_1
The capacitance of the motional (series) arm of the equivalent circuit.

Motional inductance L_1
The inductance of the motional (series) arm of the equivalent circuit.

Nominal frequency f_n
The frequency assigned by the specification of the crystal unit.

Operable temperature range
The range of temperatures as measured on the enclosure over which the crystal unit must function though not necessarily within the specified tolerances.

Operating temperature
The range of temperatures as measured on the enclosure over which the crystal unit must function within the specified tolerances.

Reference temperature
The temperature at which certain crystal measurements are made. For controlled temperature units, the reference temperature is the mid-point of the controlled temperature range. For non-controlled units the reference temperature is normally 25 ± 2 °C.

Resonance frequency f_r
The lower of the two frequencies of the crystal unit alone, under specified conditions, at which the electrical impedance of the crystal unit is resistive.

Resonance resistance R_r
The resonance of the crystal unit alone at the resonance frequency f_r.

Tolerance due to level of drive variation
The permissible deviation due to the variation of level of drive.

Tolerance over temperature range
The permissible deviation over the temperature range with respect to the frequency at the specified reference temperature.

Unwanted response
A state of resonance of a crystal vibrator other than that associated with the working frequency.

Working frequency f_w
The operational frequency of the crystal unit together with its associated circuits.

HCMOS SCHMITT TRIGGER APPLICATIONS

Digital systems often receive input signals that have long rise and fall times such as filter output signals, data-link signals, transducer output signals and signals derived from oscillators or transformers. Theoretically, the high gain between the input and output of integrated logic elements results in a rectangular output pulse regardless of the rise and fall times of the input signal. However, when a slowly rising edge of an input signal reaches the switching threshold level of the IC, it starts to switch, and charge-dumping shifts the V_{CC} and ground levels slightly. This pulls the circuit back into the pre-switching state, thereby causing a jittering output. Also, as the input signal passes slowly through the switching threshold, the power dissipation increases due to the through current in the input stage. The rise and fall times of input signals to logic systems must therefore be kept short. Furthermore, if it is necessary to construct an RC oscillator from integrated logic inverters or inverting gates, two gates or inverters (4 signal pins) must be used. To overcome these problems, the 74HC/HCT/HCU family of HCMOS logic ICs includes two ICs with Schmitt trigger inputs. They are:

- 74HC/HCT14 Hex inverting Schmitt trigger
- 74HC/HCT132 Quad two-input NAND Schmitt trigger.

The advantages of using these two ICs for waveshaping and timing are:

- in common with all HCMOS ICs, they dissipate little power and have high input impedance. The latter allows a wide range of time-constants to be used without resorting to the use of expensive high-value capacitors which would also increase power dissipation
- they have high gain, so the output is a square wave regardless of the slope of the input, but unlike with integrated gates and inverters, glitches during the transition of the input signal through the switching threshold don't cause spurious oscillations, even with the parasitic capacitance between pins
- an RC oscillator built from a Schmitt trigger requires only two pins of the IC for the signal lines. RC oscillators using gates or inverters require four signal pins
- frequency and duty factor of Schmitt trigger oscillators are largely independent of temperature because the temperature sensitivity of the trigger thresholds is only ±60 mV over the temperature range −55 °C to +125 °C
- the additional NAND function of the 74HC/HCT132 is particularly useful for enabling/disabling clock-controlled-oscillators or timing circuits.

INTERNAL CIRCUITRY AND CHARACTERISTICS

Figures 1 and 2 are the logic diagrams of the HC/HCT14 and HC/HCT132. Each input has it own Schmitt trigger that switches independently, and the inputs and outputs are buffered. The inputs also have the standard HCMOS input circuitry for protecting the inputs against ESD as illustrated in Fig.3. The HCMOS family specifications for 74HC/HCT ICs also apply to the Schmitt trigger ICs unless specified differently in the individual data sheets.

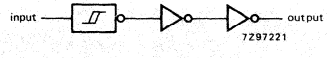


Fig.1 74HCT/HCT14 logic diagram

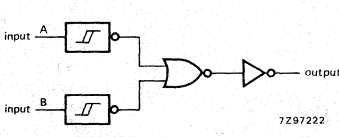


Fig.2 74HC/HCT132 logic diagram

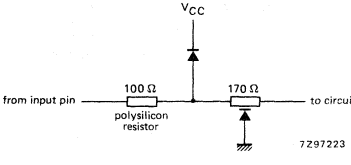
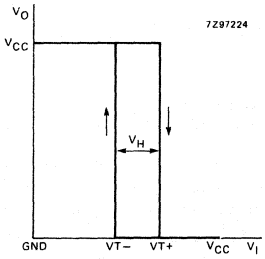
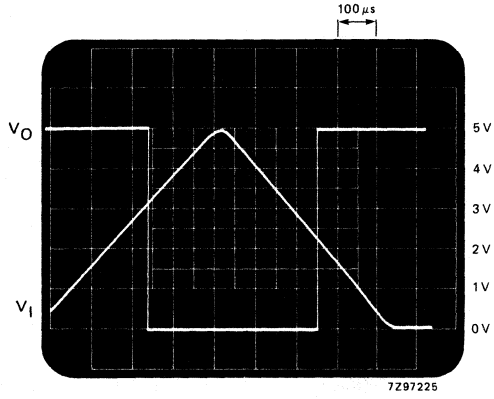


Fig.3 HCMOS input protection network

Figure 4(a) shows the transfer characteristic of a Schmitt trigger. The general shape of the characteristic is valid for all permissible values of V_{CC}, but the guaranteed maximum and minimum values of threshold voltages V_{T+} and V_{T-} are functions of V_{CC} as shown in the data sheets.



(a)



(b)

Fig.4 Schmitt trigger characteristics.
(a) transfer characteristic, (b) input and output waveforms

Figure 4(b) shows input and output waveforms illustrating the transfer characteristic of a 74HC132 Schmitt trigger with a 5 V supply and a triangular wave input. As the input voltage (V_I) increases from ground, the output remains HIGH until V_I reaches V_{T+}. At this point, the output goes LOW and remains LOW while V_I rises to V_{CC}. As V_I decreases from V_{CC}, the output remains LOW until V_I reaches V_{T-}. At this point, the output goes HIGH. By definition, the hysteresis is the difference between the HIGH tripping level (V_{T+}) and the LOW tripping level (V_{T-}).

In this example, it can be seen that V_{T+} is 3,25 V and V_{T-} is 2,25 V, giving hysteresis of 1 V. For a 74HCT Schmitt trigger, the trigger levels are lower and the minimum specified V_{T-} is 0,5 V which is less than the family specification figure of $V_{IL\,max}$ = 0,8 V for other 74HCT ICs. If a design is made with respect to the worst-case TTL-compatible input levels for 74HCT ICs ($V_{IL\,max}$ = 0,8 V and $V_{IH\,min}$ = 2,0 V), a 74HCT Schmitt trigger has less noise immunity than a 74HC type.

APPLICATIONS

Most of the applications described in this article use the 74HC/HCT132, but in circuits where both inputs are connected together, or one input is connected to V_{CC}, the 74HC/HCT14 can be used.

Waveshaping

One of the most common waveshaping applications for Schmitt triggers is in sine-to-square-wave converters like the one shown in Fig.5. The capacitive coupling removes any d.c. component from the input sine wave. The voltage divider provides a d.c. bias of $V_{CC}/2$ to allow maximum swing of the sine wave without clipping.

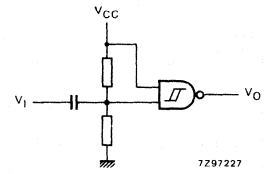


Fig.5 Sine to square-wave converter

Timing and delay

Signal delay is often provided by simple discrete RC networks. Unfortunately, if a high capacitance is used, the rise and fall-times of the delayed signal are increased considerably, causing jittering and synchronization problems. Schmitt trigger delay circuits overcome these problems since their high input-impedance allows a high-value resistor, and hence a low-value inexpensive capacitor, to be used in the RC network.

The simplest way to delay a pulse is shown in Fig.6(a). The input's leading edge is delayed by:

$$t_{d+} = RC \ln \frac{V_{CC}}{V_{CC} - V_{T+}} .$$

Its trailing edge is delayed by:

$$t_{d-} = RC \ln \frac{V_{CC}}{V_{T-}} .$$

Unfortunately, in this simple circuit, the same RC network delays both edges of the input signal (see Fig.6(b)). In many applications, only one edge has to be delayed or the edges have to be delayed by different amounts. Figure 7 shows a circuit that can delay the positive-going edge by the longest RC time and negative-going edge by the shortest RC time.

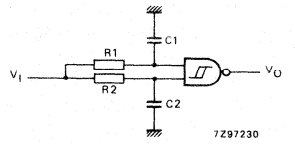
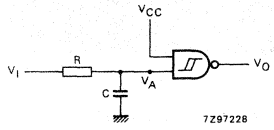
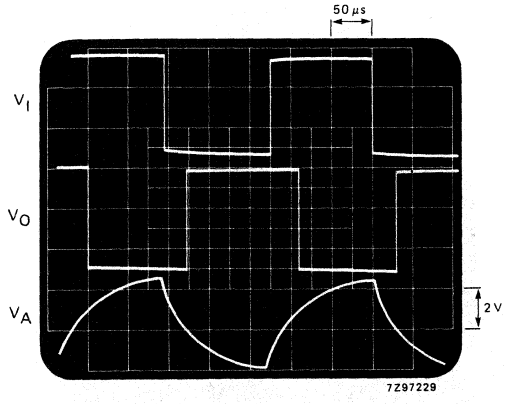


Fig.7 Circuit for delaying the positive-going and negative-going edges of an input by different amounts

If only one edge need be delayed, then the circuit shown in Fig.8 can be used to delay the positive-going edge. If the negative-going edge must be delayed, the signal must first be inverted.

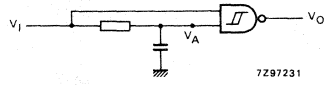


(a)

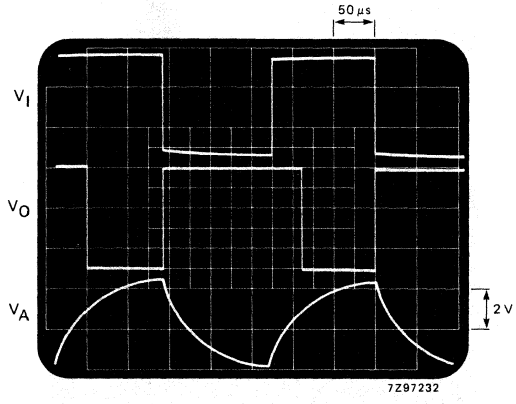


(b)

Fig.6 Delaying both edges of an input.
(a) circuit, (b) waveforms



(a)



(b)

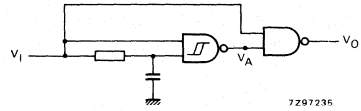
Fig.8 Delaying the positive-going edge of an input.
(a) circuit, (b) waveforms

Pulse generation

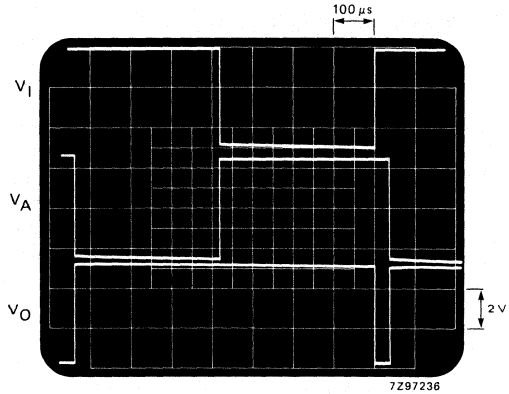
In digital systems, it is often necessary to generate an edge-triggered pulse. A circuit commonly used for this is given in Fig.9. Unfortunately, this circuit is sensitive to noise on the power-supply. If there is a spike on the supply line while the input is HIGH, a pulse with the same duration as the spike is transmitted from the output of the previous stage via the input capacitor. So, it's better to use the circuit shown in Fig.10 which, although more complex, has higher noise-immunity.

Oscillators

The circuit of a simple relaxation oscillator is given in Fig.11. The second input of the 2-input NAND Schmitt trigger HC/HCT132 can be used as an enable/disable for the oscillator. This is often required in battery-powered equipment to set an oscillator to the 'standby' mode to reduce power consumption.

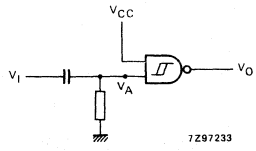


(a)

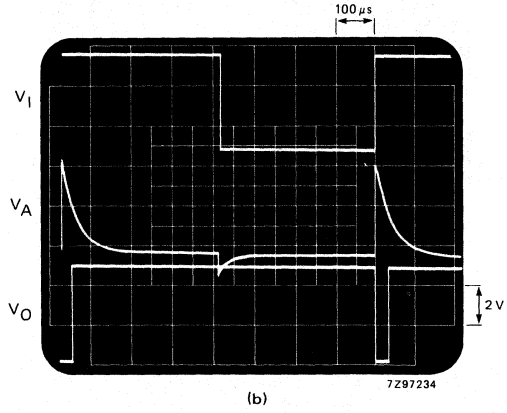


(b)

Fig.10 Preferred method of generating a pulse coincident with the positive-going edge of the input signal. (a) circuit, (b) waveforms

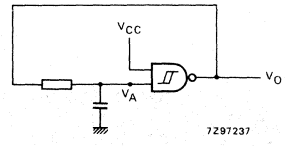


(a)

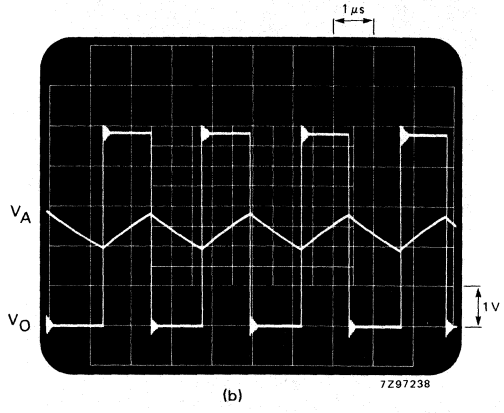


(b)

Fig.9 Generating a pulse coincident with positive-going edge of the input signal. (a) circuit, (b) waveforms



(a)



(b)

Fig.11 Relaxation oscillator with a duty factor of 0,5. (a) circuit, (b) waveforms

The HIGH and LOW periods (t_1 and t_2) for the oscillator are:

$$t_1 = RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$t_2 = RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_1 + t_2 = RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})} .$$

These formulae are only valid if the value of the resistor is high-enough to ensure that the output voltage drop is negligible. This must be checked against the family specification.

As the Schmitt-trigger input swings between V_{T+} and V_{T-} (the linear region of operation), the through-current I_{CC} in the input stage is maximum. The average through current and its power dissipation are indicated in Table 1. Although this power dissipation during switching is usually higher than that of an RC oscillator using HCMOS gates or inverters, this circuit does have the important advantage of only requiring two pins for the signal connections.

The frequency and duty factor of this oscillator depend on the ratio V_{T+}/V_{T-}. Since this ratio remains almost constant with supply voltage variations, these have little influence on the duty factor or frequency. However, since the ratio V_{T+}/V_{T-} varies with switching level spreads between ICs, the influence of these on the duty factor and frequency can be considerable. The resistor in the RC network should therefore be made adjustable to compensate for switching level spreads between individual ICs.

The frequency of the oscillator as a function of supply voltage with RC time as a parameter is shown in Fig.12.

TABLE 1
Power dissipation due to average through current during switching

type	V_{CC} (V)	power dissipation (mW)	average through-current (μA)
74HC14	2	0,096	48
	4,5	2,16	480
	6,0	5,3	880
74HC132	2,0	0,08	40
	4,5	1,85	410
	6,0	4,44	740

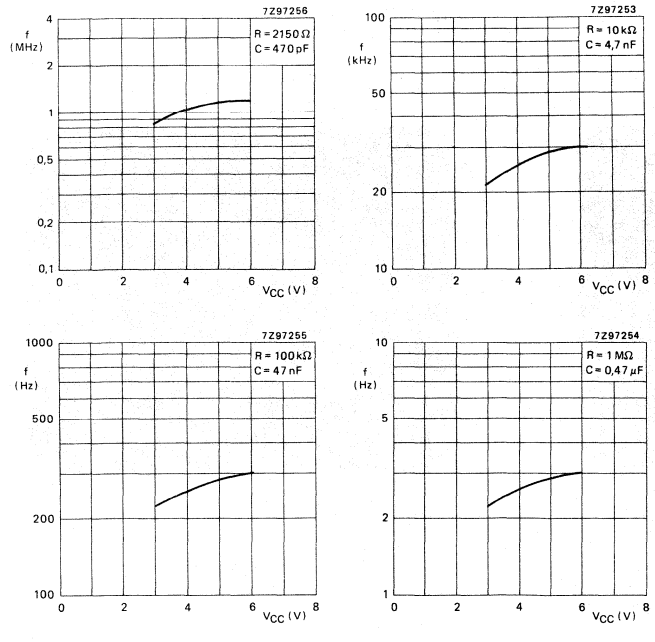
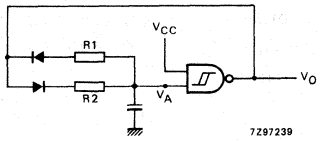
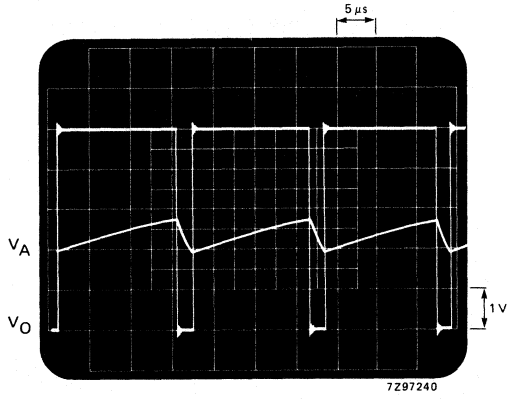


Fig.12 Frequency as a function of supply voltage with time-constant as a parameter for Schmitt trigger RC oscillators according to the circuit of Fig.11



(a)



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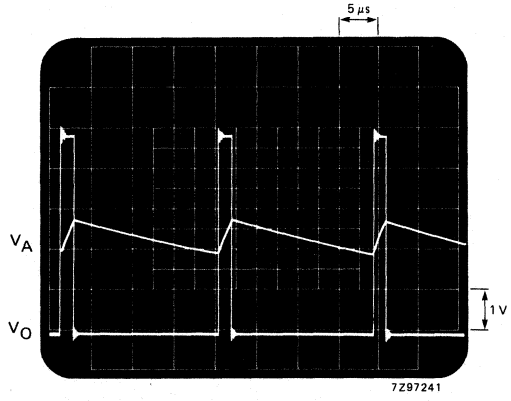


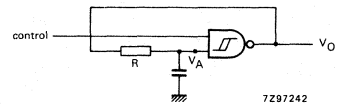
(c)

Fig.13 Relaxation oscillator with unequal HIGH and LOW periods. (a) circuit, (b) operation with HIGH period much longer than LOW period, (c) operation with LOW period much longer than HIGH period

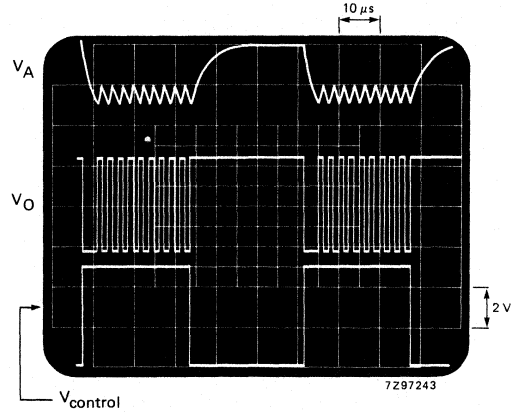
The duty factor is 0,5 when the tripping levels (V_{T+} and V_{T-}) are symmetrical about $V_{CC}/2$. The waveforms in Fig.11 illustrate that, in this example, the duty factor is almost 0,5. To obtain a duty factor of exactly 0,5, the oscillator can be run at twice the frequency and its output divided by a flip-flop.

Another way to alter the duty factor is to use the circuit in Fig.13(a). With this arrangement, the LOW and HIGH periods are individually set by resistors R_1 and R_2 respectively. In Fig.13(b), the HIGH period is much longer than the LOW period ($R_2 > R_1$), and in Fig.13(c), the LOW period is much longer than the HIGH period ($R_1 > R_2$). A controlled Schmitt trigger oscillator can also be designed as shown in Fig.14. Note that the first LOW period is considerably longer than subsequent LOW periods. This is because the capacitor's initial charge is higher. The duration of the first LOW period is:

$$t = RC \ln \frac{V_{CC}}{V_{T-}} .$$



(a)



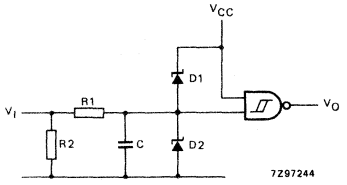
(b)

Fig.14 Controlled relaxation oscillator. (a) circuit, (b) waveforms

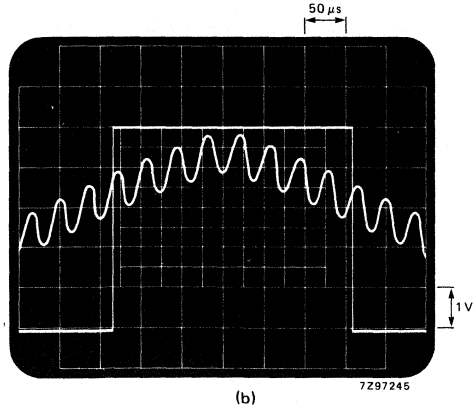
Input filtering

Input signals to digital systems are often very noisy. This problem can be solved with an input filter made with a Schmitt trigger as shown in Fig.15.

Resistor R_2 can also be a pull-up resistor connected to V_{CC} if this suits the system better. The time-constant chosen depends on the amount of noise and on the permissible speed reduction. The two diodes should be Schottky types (e.g. BAT85). They ensure that the current through the internal input protection diodes does not exceed the maximum rating. Figure 15(b) illustrates the effectiveness of this filter by comparing its output with its input.



(a)



(b)

Fig.15 Input filter for noisy signals.
(a) circuit, (b) waveforms

CIRCUIT DESIGN CRITERIA

Family specification

All circuit calculations must be based on the guaranteed parameters given in the 74HC/HCT/HCU family specification. However, no specific parameters are given for oscillators. This is because external components define the performance of the oscillator. The values of these components must therefore be calculated from the data in the family specification to ensure that input/output currents and maximum dissipation are not exceeded.

Value limits for timing resistors

For predictable operation, the minimum values for timing resistors are dictated by the output drive available. For the 74HC132 with a supply voltage of 4,5 V, $V_{OL\,max}$ and $V_{OH\,min}$ are 0,4 and 3,7 V respectively, with an output current of 4 mA. Also, $V_{T+\,max}$ is 3,15 V and $V_{T-\,min}$ is 0,9 V. The minimum value for the timing resistor when the output is LOW is:

$$R_{min} = \frac{V_{T+\,max} - V_{OL\,max}}{I_{OL}} = \frac{3,15 - 0,4}{0,004} = 688\,\Omega.$$

When the output is HIGH, the minimum value for the timing resistor is:

$$R_{min} = \frac{V_{T-\,min} - V_{OH\,min}}{I_{OH}} = \frac{0,9 - 3,7}{0,004} = 700\,\Omega$$

For this example, R_{min} at $V_{CC} = 4,5$ V is therefore 700 Ω. To keep the voltage drop due to leakage current low, the maximum value for timing resistors is 1 MΩ.

Power dissipation due to through-current in the input stage

Figure 16 shows the typical power dissipation ($V_{CC}I_{CC}$) due to through current in the first stage for the 74HC14 and 74HC132 Schmitt triggers as a function of supply voltage. The power dissipation is almost frequency-independent up to 25 kHz, but above this frequency there is a slight increase. By 2 MHz the power dissipation has doubled.

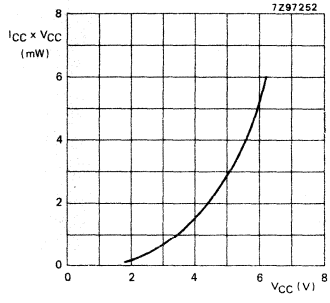


Fig.16 Typical power dissipation due to through-current in the first stage for the 74HC/HCT14 and 74HC/HCT132 Schmitt trigger as a function of supply voltage

Total power dissipation

The total power dissipation consists of:

$$P_{osc} = fC_tV_H^2 + fV_{CC}^2 (C_{PD} + C_L) + V_{CC}I_{CC}$$

where:

- V_H = hysteresis ($V_{T+} - V_{T-}$)
- f = frequency
- V_{CC} = supply voltage
- C_t = the timing capacitance
- C_{PD} = the equivalent device power dissipation capacitance given in the data sheets
- C_L = the output load capacitance
- I_{CC} = the average through current when the input swings between V_{T+} and V_{T-}. It is proportional to $(0{,}5V_{CC} - 0{,}7\ V)^2$. The average through currents for the 74HC14 and 74HC132 used as RC oscillators are shown in Table 1 and Fig.16.

Maximum oscillator frequency

To avoid propagation delay effects, the frequency of oscillators should be kept well below:

$$f_{osc\,max} = \frac{1}{t_{PHL} + t_{PLH}}$$

where:

t_{PHL} = the propagation delay for a HIGH to LOW transition

t_{PLH} = the propagation delay for a LOW to HIGH transition.

USING 74HCT HCMOS TO REPLACE LSTTL AND DRIVE TRANSMISSION LINES

Before the introduction of our 74HC/HCT/HCU high-speed CMOS (HCMOS) family of logic ICs, designers of high speed logic systems were restricted to the use of power-hungry bipolar ICs such as LSTTL. Since the logic ICs of the HCMOS family can operate as fast as LSSTL but consume much less average power, and since they can operate over a wider supply voltage range, using them to replace LSTTL results in considerable system economies for both new and existing logic system designs. HCMOS ICs with the suffix 74HCT are purpose-designed for the latter application. Not only are they pin- and function-compatible with their LSTTL counterparts, they also have TTL-compatible input voltage levels and the same fanout as LSTTL (10 LSTTL loads). They can therefore be simply inserted in place of bipolar LSTTL logic ICs of the same type without the need for any redesign to achieve wider noise margins. What's more, they dissipate much less power, are more reliable and allow the use of simpler power supplies and cooling arrangements than those required for LSTTL. This article compares the input/output structures and performance of LSTTL and 74HCT logic ICs and discusses interfacing and low-power techniques for driving terminated data transmission lines with 74HCT ICs.

INPUT/OUTPUT CHARACTERISTICS OF LSTTL AND 74HCT ICs

Input characteristics

The input structure of 74HCT ICs is shown in Fig.1(a). The resistor/diode network protects the input against electrostatic discharge by clamping input voltages which exceed the supply rails to V_{CC} or ground. Under normal operating conditions, the input voltage should swing within the supply voltage limits (V_{CC} and ground) to prevent current flow through diodes D_1 and D_2. The maximum permitted d.c. through these diodes is 20 mA.

If MOS transistors P1 and N1 were identical they would have a switching threshold of $V_{CC}/2$ (as in 74HC ICs). A minimum HIGH level derived from an LSTTL output (2,7 V), although being recognized as a logic "1" would then allow both input transistors to partially conduct, causing a flow-through current between V_{CC} and ground, thus increasing power dissipation. To prevent this, N1 is enlarged in 74HCT ICs and level shifting diode D3 is incorporated between the drain of P1 and V_{CC}. The effect of D3, combined with N1 having higher gain than N2, is to reduce the input switching threshold to 1,4 V typical which matches that of LSTTL. Unlike LSTTL inputs however, 74HCT inputs present a purely capacitive load to a driving IC and therefore draw only a small leakage current when quiescent. The maximum leakage current into 74HCT inputs held in the HIGH or LOW state is only 1 μA. This is essentially zero when compared to the input current of LSTTL which is 400 μA in the LOW state and 20 μA in the HIGH state.

The main consequence of 74HCT inputs having a much higher impedance than LSTTL inputs is, of course, a considerable reduction of power dissipation which simplifies power supplies, cooling arrangements and battery back-up. A drawback however is that a 74HCT input creates a high impedance termination for a transmission line. This will cause reflections and consequent corruption of data unless the line is terminated with its characteristic impedance formed by a discrete termination network. This is explained in more detail in the Appendix.

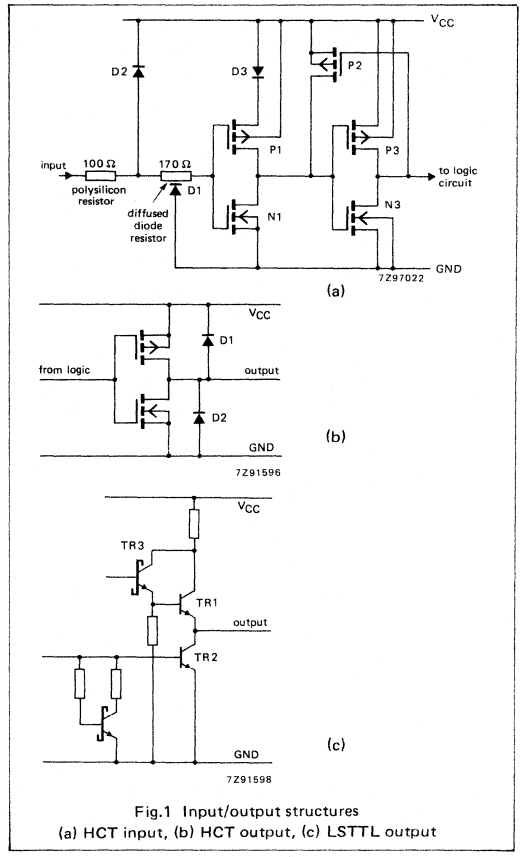


Fig.1 Input/output structures
(a) HCT input, (b) HCT output, (c) LSTTL output

Output characteristics

The output structure of a 74HCT IC is shown in Fig.1(b). With an output current of 20 μA, the LOW to HIGH output level swing is from 0,1 V to V_{CC} – 0,1 V. With an output current of 4 mA (6 mA for bus drivers) $V_{OH\,min}$ is 0,66 V below V_{CC}, and $V_{OL\,max}$ is 0,33 V. Figure 2 shows that, when a 74HCT output is at worst-case LSTTL output levels (V_{OH} = 2,7 V min. and V_{OL} = 0,5 V max.), it can source 8 mA (12 mA for bus drivers) and sink 6 mA (9 mA for bus drivers) with a 4,5 V supply.

In contrast, the HIGH output level for the LSTTL output structure shown in Fig.1(c) is limited by the V_{BE} of TR_1 and TR_3 and the voltage drop across the collector resistor. Over the full temperature range, V_{OH} can therefore be as low as 2,7 V at $I_{OH\,max}$ with the minimum supply voltage (4,75 V). The LOW output level for LSTTL is the saturation V_{CE} of TR_2. Even if a source current flows out of the output, V_{OL} will not exceed 0,5 V.

The main consequence of 74HCT ICs having a wider output voltage swing than LSTTL ICs is that the noise immunity of a 74HCT logic system is much greater than that of a comparable LSTTL system.

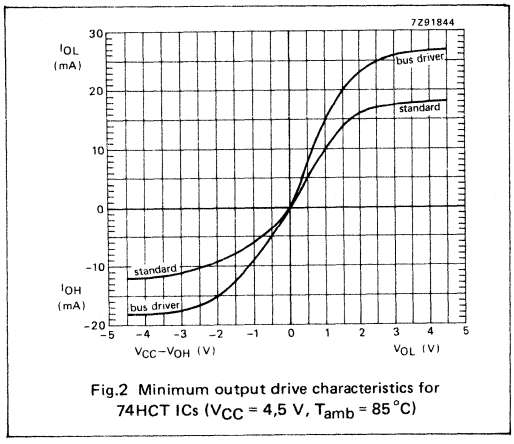


Fig.2 Minimum output drive characteristics for 74HCT ICs (V_{CC} = 4,5 V, T_{amb} = 85 °C)

PERFORMANCE COMPARISON

Of paramount importance for the replacement of LSTTL ICs with 74HCT types is the identical input voltage specifications and nominal operating voltage for the two technologies. The maximum LOW input level is 0,8 V; the minimum HIGH input level is 2 V. The nominal operating voltage is 5 V.

The Table compares all applications-related parameters of 74HCT and LSTTL ICs. The following comparisons which are based on the figures in the Table show that 74HCT ICs not only easily replace LSTTL ICs, they also enhance system performance in many respects.

Quiescent power dissipation

The quiescent power dissipation of 74HCT ICs is due only to small leakage currents flowing between V_{CC} and ground and is essentially zero compared with that of LSTTL ICs. However, when a 74HCT input is driven by a TTL minimum HIGH level of (V_{CC} – 2,1 V), a small current is drawn from V_{CC}. This current is called additional quiescent supply current (ΔI_{CC}) and is specified on a per input basis in the d.c. characteristics for HCT ICs. Since all LSTTL ICs (except some bus drivers) have a higher minimum HIGH level (2,7 V) than TTL ICs, the published figures for the additional quiescent supply current can be halved when 74HCT ICs are driven by LSTTL.

Dynamic power dissipation

Unlike the dynamic power dissipation of LSTTL, the dynamic power dissipation of 74HCT ICs is due to the charge and discharge of capacitive loads and is therefore frequency-dependent. It is only comparable to that of LSTTL ICs at high operating frequencies. Generally, it is much lower because average data transmission rates are less than 1 MHz. A full discussion on 74HC/HCT power dissipation and how to calculate it is given in the section Power Dissipation.

Supply voltage

74HCT ICs need much less voltage regulation than LSTTL ICs. They operate from a nominal supply of 5 V, the same as LSTTL. The permitted supply voltage deviation from the nominal value for 74HCT (±10%) is twice as much as that for LSTTL (±5%).

Operating temperature range

The operating temperature range for 74HCT ICs is –40 °C and +125 °C. This is less limiting than the 0 °C to +70 °C specified for 74LSTTL.

Noise immunity

Replacing LSTTL with 74HCT can considerably increase the noise immunity of a logic system. For a totally 74HCT system with a 4,5 V supply, the noise margins are 53% of V_{CC} (HIGH) and 14% of V_{CC} (LOW) with one 74HCT output driving 20 74HCT inputs. For an LSTTL system with a 4,75 V supply they are 15% of V_{CC} (HIGH) and 8% of V_{CC} (LOW). However, if the full drive capability of 74HCT bus logic is exploited (driving a d.c. terminated transmission line for example), the 74HCT output levels will be the same as those for LSTTL and the noise immunity will also be the same.

Comparison of characteristics of 74HCT and LSTTL circuits (V_{CC} = 5 V unless stated otherwise)

characteristic		74HCTXXX			74LSXXX	
max. quiescent power dissipation over temp. range at V_{CC} max						
per gate (mW)		0,027			6	
per flip-flop (mW)		0,11			22	
per 4-stage counter (mW)		0,44			175	
per transceiver/buffer (mW)		0,055			60	
max. dynamic power dissipation (C_L = 50 pF)						
at f_i (MHz)	*0,1*	*1*	*10*	*0,1 to 1*		*10*
per gate (mW)	0,25	2,25	22	6		22
per flip-flop (mW)	0,35	2,5	24	22		27
per 4-stage counter (mW)	0,70	3	27	175		200
per buffer/transceiver (mW)	0,30	2,5	24	60		90
operating supply voltage (V)		4,5 to 5,5			4,75 to 5,25	
operating temperature range (°C)		−40 to +85 −40 to +125			0 to +70	
max. noise margin (H/L in V)		2,9/0,7			0,7/0,4	
input switching voltage stability over temp. range		±60 mV			±200 mV	
min. output drive current at T_{max} and $V_{CC\,min}$ (mA) source current (V_{OH} = 2,7 V)*						
standard logic		−8			−0,4	
bus logic		−12			−2,6	
sink current						
standard logic (V_{OL} = 0,4 V)		4			4	
standard logic (V_{OL} = 0,5 V)		6			8	
bus logic (V_{OL} = 0,4 V)		8			12	
bus logic (V_{OL} = 0,5 V)		9			24	
typ. output transition time (ns) (C_L = 15 pF) standard logic						
t_{TLH}		6			15	
t_{THL}		6			6	
bus logic						
t_{TLH}		4			15	
t_{THL}		4			6	
typ. propagation delay (ns) (C_L = 15 pF)**						
gate t_{PHL}/t_{PLH}		8/8			8/11	
flip-flop t_{PLH}		14			15	
flip-flop t_{PHL}		14			22	
typ. clock rate of a flip-flop (MHz)		50			33	
max. input current (μA)						
I_{IL}		−1			−400 to −800	
I_{IH}		1			40	
3-state output leakage current (μA)		±5			±20	

* V_{OH} for a few LSTTL bus outputs is specified as 2,4 V.
** Refer to data sheets for the effect of capacitive loading.

Stability of input switching threshold

The switching threshold of the input pair of CMOS transistors in 74HCT ICs (1,4 V) is the same as that of LSTTL but it is less temperature dependent than that of the diode input circuitry of LSTTL. The noise margin of 74HCT ICs therefore remains more stable over the operating temperature range. RC astable multivibrators are also less susceptible to temperature variations.

Timing

The sizes of the p-channel/n-channel MOS transistors in the push-pull output stages of 74HCT ICs are adjusted to obtain saturation currents which result in equal output transition times ($t_{TLH} = t_{THL}$). The sizes of the p-channel/n-channel MOS transistors in all the symmetrical logic circuitry stages are adjusted to obtain equal propagation delays ($t_{PHL} = t_{PLH}$).

Maximum clock frequency

The maximum clock frequencies of 74HCT ICs are comparable to those of equivalent LSTTL ICs.

Input current

An important difference between systems using LSTTL and 74HCT ICs is the relatively high constant direct current that flows in LSTTL interconnect wiring. In comparison, the current flowing into 74HCT inputs is essentially zero. Typically, only a few pA of reverse current flows in the input diodes. This results in better buffering and a wider frequency range for RC oscillators and time delay circuits constructed from 74HCT ICs.

Leakage current of 3-state outputs

Since the leakage current of the 3-state outputs of 74HCT bus drivers in the high-impedance state is only a quarter that of LSTTL circuits, the values of pull-up/pull-down resistors for bus drivers with 3-state outputs can be increased to reduce power dissipation.

Output drive current

The guaranteed minimum source current for HCT ICs is much higher than that of LSTTL and is matched to the sink current to achieve balanced L/H and H/L transition times. The sink current of 74HCT ICs is lower than that of LSTTL ICs to minimize current spiking and electromagnetic radiation, but is sufficient for LSTTL interfacing requirements. This article discusses the influence of the lower sink current and higher input impedance of 74HCT ICs on line terminations; the only area of logic system design which may be affected when replacing LSTTL ICs with 74HCT equivalents.

LSTTL/HCT INTERFACING

The following worst-case figures are based on systems with a single nominal 5 V supply and using standard logic with each output driving ten inputs.

Driving 74HCT from LSTTL

The LSTTL output/74HCT input levels for a worst-case single supply voltage (4,75 V) are:

LSTTL	*74HCT*
V_{OL} max = 0,4 V	V_{IL} max = 0,8 V
V_{OH} min = 2,7 V	V_{IH} min = 2 V.

This allows direct interfacing. The maximum current flowing into each 74HCT input is only 1 μA. This means that the 74HCT input structure presents a true CMOS type d.c. load resulting in a high fanout. The HIGH and LOW noise margins will be the same as those for an all LSTTL system.

Driving LSTTL from 74HCT

The 74HCT output/LSTTL input levels for a worst-case single supply voltage (4,75 V) are:

74HCT	*LSTTL*
V_{OL} max = 0,33 V	V_{IL} max = 0,8 V
V_{OH} min = 4,1 V	V_{IH} min = 2 V.

This again allows direct interfacing. The LOW level noise margin will be 70 mV greater than that for an all LSTTL system, and the HIGH level noise margin will be 1,4 V greater.

Driving 74HCT from 74HCT

The 74HCT output/input levels for a worst-case single supply voltage (4,5 V) are:

74HCT output	*74HCT input*
V_{OL} max = 0,1 V	V_{IL} max = 0,8 V
V_{OH} min = 4,4 V	V_{IH} min = 2 V.

The LOW level noise margin will be 0,3 V greater than that with LSTTL, and the HIGH level noise margin will be 1,7 V greater.

74HCT to 74HCT drive capability is expressed as minimum guaranteed source/sink current at a specified output voltage as shown in Fig.2. Since a quiescent 74HCT input draws a maximum of 1 μA, the unit-load (UL) concept as used for LSTTL doesn't apply. Instead, consideration must be given to charging/discharging capacitive loads. With a specified LOW output level of 0,33 V, a standard logic 74HCT output can sink 4 mA which is equivalent to driving 4000 74HCT inputs. Even with a specified low output level of 0,1 V, a standard output can still sink 20 μA which means that it can drive twenty 74HCT inputs.

TERMINATION OF UNUSED INPUTS

Termination of unused LSTTL inputs is not absolutely necessary because all inputs have an internal pull-up of 2200 Ω. However, if good design practice has been followed, all unused inputs of LSTTL ICs will be terminated to prevent any possibility of linear operation of the input circuitry which would considerably increase power consumption. Unlike LSTTL inputs, the impedance of 74HCT inputs is very high and, if unused, they must be terminated to prevent the input circuitry floating into the linear mode of operation which would cause extra supply current flow or oscillation. Unused 74HCT inputs can be terminated by connecting them to V_{CC} or ground, either directly, or via resistors of between 1 kΩ and 1 MΩ. Since the value of terminating resistors for unused inputs of LSTTL ICs is usually between 220 Ω and 1,2 kΩ, it will often be possible to directly replace LSTTL circuits with their 74HCT counterparts.

SUPPLY DECOUPLING

General requirements for power supply decoupling are discussed in the User Guide section. In any circuitry for driving terminated lines, the supply to each IC must be decoupled to ground by a ceramic capacitor of at least 10 nF. The capacitor should be as close as possible to the ground pin of the IC to minimize inductance which could cause ringing in the ground of the IC. If ringing persists when a 74HCT IC is driving a terminated line, and this ringing or noise is above or near the input switching threshold (1,4 V), the receiving IC should be replaced with an HC type which has a higher input switching threshold ($V_{CC}/2$) than 74HCT or LSTTL ICs.

In critical applications where hardly any noise can be tolerated, the supply to the circuit board or card can be decoupled by a low-pass RC filter consisting of a 10 Ω or lower value resistor of adequate power rating in series with the supply to the ICs and a 33 μF or higher value capacitor in parallel with the supply input. This filter should be at the point where the supply voltage enters the board or card.

DRIVING DATA LINES

Printed circuit-board tracks or striplines are used to carry data on circuit-boards, but twisted pairs of wires and coaxial cables are often used to carry data over longer distances in a system or in a large backplane. The lines are considered to be electrically long and will behave as transmission lines if the time taken for a transition to travel the length of the line and return exceeds the rise or fall time of the transition. If an electrically long line is not terminated with its characteristic impedance (for example, with the inputs of 74HCT ICs, which have a much higher impedance than those of LSTTL ICs), reflections will occur and cause ringing which can corrupt high speed data. This is explained in more detail in the Appendix.

Driving a pcb track multi-transistor data bus

One of the major uses of logic ICs is in computer and microprocessor-based systems incorporating transceivers, octal latches, and line drivers with 3-state outputs connected to a data bus consisting of a pcb track. The 3-state outputs allow several driver ICs to be connected to the same bus because they remain in the high-impedance state when inactive.

Even if a 3-state 74HCT bus isn't long enough to act as a transmission line, it must be terminated with a pull-up/pull-down resistor to prevent noise pick-up if it remains in the high-impedance state for more than 100 μs. However, it is good practice to always terminate a 3-state bus in case the system stops momentarily in the high impedance state or there is noise in the system due to crosstalk. Choice of either a pull-up or pull-down resistor will depend on whether a HIGH or LOW state is required on the bus during the high impedance state. Choice of the resistor value is a compromise between power dissipation and bus speed. A higher resistance will reduce power dissipation but will increase the time-constant in conjunction with the bus capacitance and increase the time needed for pull-up/pull-down. A lower resistance will speed up the bus will dissipate more power. Typical values of pull-up resistors are 220 Ω to 1,2 kΩ for LSTTL and 750 Ω to 1 MΩ for 74HCT. Typical values of pull-down resistors are 680 Ω to 1 kΩ for LSTTL and 1 kΩ to 1 MΩ for 74HCT. Pull-up/pull-down resistors should be positioned as far as possible from the bus drivers. Multiple terminating resistors can be distributed along the bus, but their individual values must then be high enough to ensure that the total parallel pull-up or pull-down resistance is not less than the values previously mentioned.

Driving a stripline multi-transmitter data bus

The propagation delay along a stripline on a glass-epoxy pcb is 7,2 ns/m. With rise and fall times of 4 ns, the bus is considered to be electrically long if it exceeds 28 cm. In the unlikely event of a 3-state pcb wiring bus with multiple drivers being much longer than this, it must consist of a stripline terminated at both ends by its characteristic impedance to prevent reflections corrupting the transmitted data (see Appendix). Such a stripline usually consists of a 0,6 mm track on one side of a 1,6 mm thick glass-epoxy pcb and a groundplane on the other. This has a

characteristic impedance of 120 Ω. An arrangement for terminating this type of bus for LSTTL circuits is shown in Fig.3. The output of the LSTTL driver has to sink 47 mA at a V_{OL} of 0,5 V, and the total power dissipated by the driving IC and the terminating network in the LOW state is more than 250 mW.

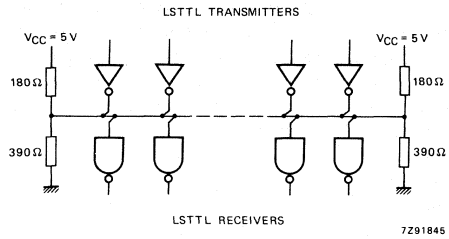
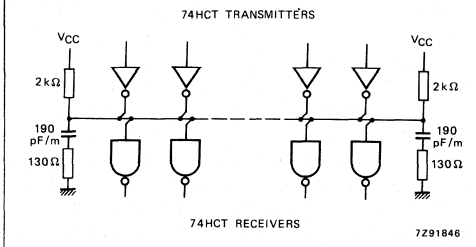


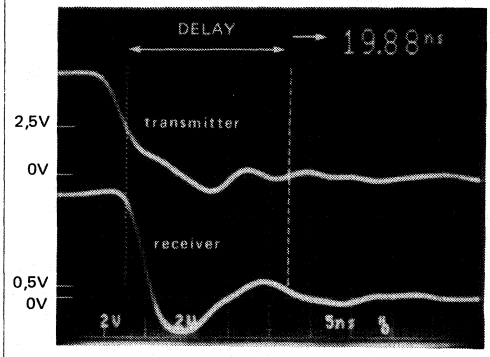
Fig.3 A d.c. termination for a stripline data bus with several 3-state LSTTL drivers

74HCT bus drivers cannot be used to replace LSTTL ICs driving a 120 Ω stripline more than 28 cm long in the arrangement of Fig.3 because:

- the required sink current (47 mA) far exceeds the guaranteed minimum sink current of 10 mA specified at V_{OL} = 0,5 V for a 74HCT bus driver
- total power dissipation of more than 250 mW per driver (including dissipation in the termination network) is contrary to the principle of replacing LSTTL ICs with 74HCT types to reduce power dissipation
- with a supply of 4,5 V, a V_{OL} of 0,5 V, $I_{OL\,max}$ = 9 mA, a terminating arrangement like the one shown in Fig.3 and the same ratio of resistor values (2:1), the lowest impedance line terminated at both ends that can be driven by a 74HCT bus driver is about 500 Ω (two 500 Ω terminations in parallel = 250 Ω effective load). A characteristic impedance of 500 Ω is impractical for a stripline.

However, resistive (d.c.) termination of an electrically long stripline multi-transmitter data bus is not essential because, as shown in the Appendix, the line can instead be terminated with its characteristic impedance (120 Ω) consisting of a series RC network (HCT bus drivers can deliver up to 70 mA during switching). A suitable low-power termination for a 3-state bus is shown in Fig.4. The maximum d.c. power dissipation of this arrangement when the bus is in the LOW state is only 21 mW. The network shown provides a pull-up facility when the bus is in the high-impedance state.





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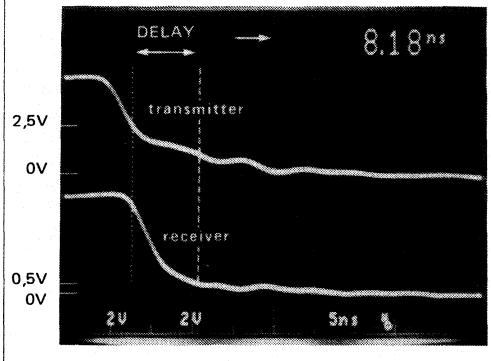

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Fig.4 An a.c. termination with pull-up for a stripline data bus with several 3-state 74HCT drivers

Driving twisted wire lines

Another type of line that must often be driven in logic systems consists of a pair of 0,38 mm (28 SWG) pvc-insulated wires twisted together. One of the wires is grounded and the characteristic impedance of the line is 110 Ω. The propagation delay along a twisted wire line is 6,2 ns/m. With rise and fall times of 4 ns, the line is considered to be electrically long if it exceeds 32 cm. Since it can only be end-driven, termination is only required at the receiving end of the line.

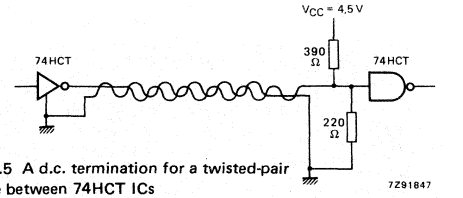


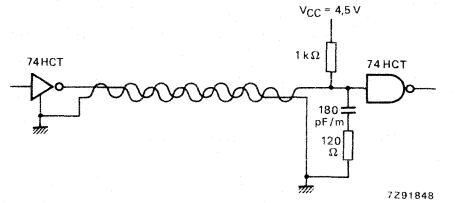
Fig.5 A d.c. termination for a twisted-pair line between 74HCT ICs

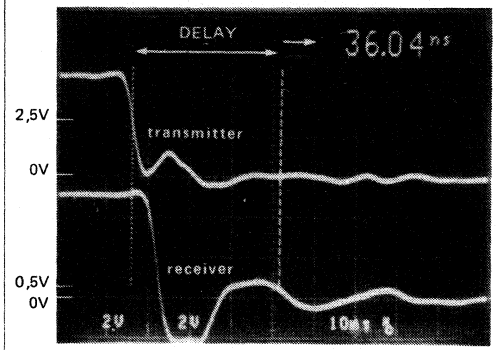
A twisted wire line driven by a 74HCT driver cannot be terminated with a 2:1 resistive potential divider with an effective parallel resistance of 110 Ω without exceeding the minimum guaranteed sink and source currents. By changing the potential divider ratio to 3:2 however, a 140 Ω termination can be made as shown in Fig.5. The total d.c. power dissipation (driver output plus termination network) in the LOW state is 42 mW.

A low-power 110 Ω a.c. termination suitable for the receiving end of a twisted wire line which requires pull-up/pull-down is shown in Fig.6. The capacitor has a low impedance to reflections and its value is calculated from the information in the Appendix. The total d.c. power dissipation of this arrangement in the LOW state is 17 mW. If a pull-up/pull-down facility is not required (2-state line), the 1 kΩ resistor can be omitted and the value of the remaining resistor reduced to 100 Ω. The d.c. power dissipation will then be reduced to zero.

Driving coaxial cables

Another type of data link is coaxial cable. There are various types of coaxial and triaxial cable available, but the most commonly used is RG-59B/U which has a characteristic impedance of 75 Ω and a propagation speed of 5 ns/m. With rise and fall times of 4 ns, the cable is considered to be electrically long if it exceeds 40 cm. One of the most common terminations used when driving a long coaxial cable with an LSTTL IC is shown in Fig.7. Since this termination provides a poor impedance match, requires a current sinking capability of about 20 mA and dissipates 100 mW in the LOW state, a 74HCT bus driver can't be used to drive it without exceeding its minimum guaranteed sink current.





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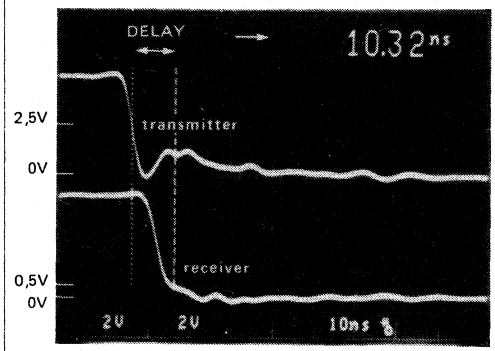

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Fig.6 A low-power a.c. termination for a twisted-pair line between 74HCT ICs

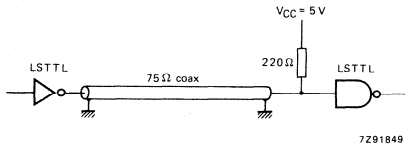


Fig.7 Termination of a 75 Ω coaxial cable interconnecting LSTTL ICs

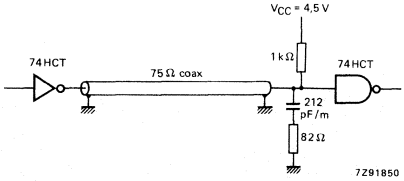


Fig.8 An a.c. termination with pull-up for a 75 Ω coaxial cable between 74HCT ICs

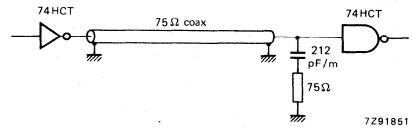
If pull-up/pull-down is required, it is therefore necessary to use an a.c. line termination with pull-up as shown in Fig.8. If pull-up/pull-down is not required (2-state line), the low-power a.c. termination shown in Fig.9 can be used. The coaxial cable should be terminated with its characteristic impedance at both ends for cable runs of more than 15 m.

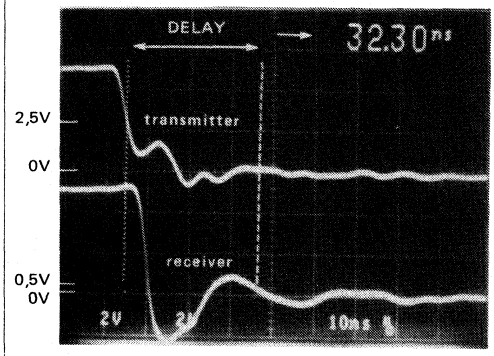
Driving ribbon cable

The risk of crosstalk between the high impedance 74HCT inputs due to capacitive and inductive coupling is an additional factor restricting the length of unterminated ribbon cable that can be connected between 74HCT ICs. When the connections act as transmission lines the problem becomes even more critical. Since it is extremely difficult to calculate the combined effects of crosstalk and reflections in ribbon cable, the length restrictions are best determined empirically.

The length of an unterminated ribbon cable with a signal on each wire should not exceed 60 cm. If each alternate wire in the ribbon is grounded as shown in Fig.10, the unterminated length limit increases to 1,8 m.

A 74HCT IC can drive a longer ribbon cable if each signal wire is terminated with a pull-up resistor, pull-down resistor or one of the twisted-pair terminations previously described. With a 1 kΩ pull-up resistor per wire and no alternate ground wires, the maximum length that can be driven without crosstalk causing problems is 120 cm. The same arrangement but with alternate wires grounded as shown in Fig.11 increases the maximum permitted length to 2 m. When using a twisted-wire line a.c. termination with a Thévenin impedance of 170 Ω, but not using an alternate ground scheme (Fig.12), the maximum length





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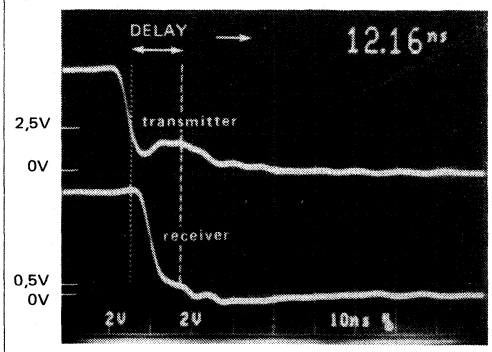

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Fig.9 A low-power a.c. termination for a 75 Ω coaxial cable

that can be driven is 2 m. By adding the alternate grounded wires, the maximum length is extended to 5 m. The maximum length of ribbon cable that can be driven can be extended beyond 5 m by using 170 Ω terminations at both ends of the cable. The main point to bear in mind is that the maximum guaranteed sink current as specified for 74HCT ICs in the Table at the beginning of this article must never be exceeded.

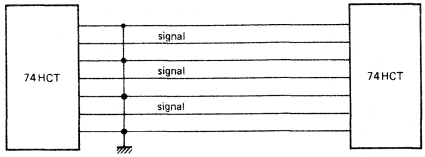


Fig.10 Unterminated ribbon cable with alternate ground wires

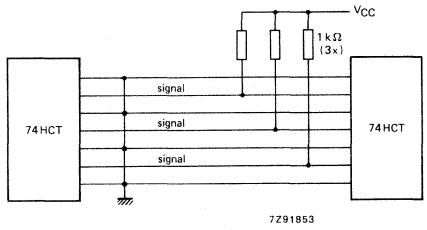
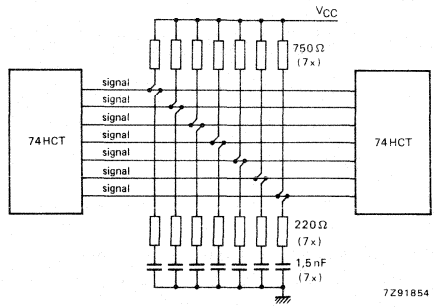
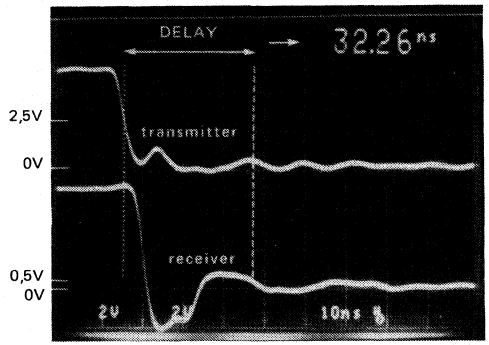


Fig.11 Ribbon cable with alternate ground wires and pull-up resistors





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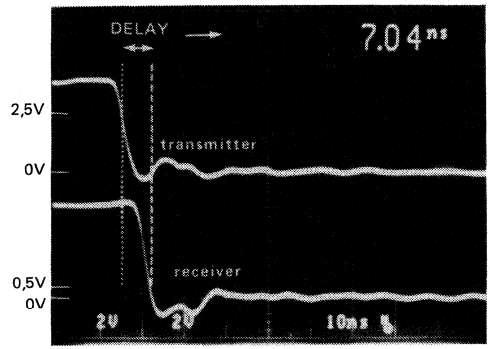

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Fig.12 Ribbon cable terminated with an impedance of 170 Ω

APPENDIX

TRANSMISSION LINE REFLECTIONS AND TERMINATIONS

In digital systems, an interconnection is considered to be electrically long when the time taken for a transition to propagate down the line and return exceeds the rise or fall time of the transition. Such a line cannot be regarded as a short-circuit between the points it connects (with stray capacitance to ground), but must be regarded as a transmission line with characteristic impedance Z_O. A fast switching edge transmitted along an incorrectly terminated transmission line will be reflected by the line termination, possibly several times, before a steady state is reached. These reflections can degrade system performance by introducing delays and causing spurious switching.

If the input impedance of the line receiver and the output impedance of the line driver at $(V_{OH} - V_{OL})/2$ are both higher than the characteristic impedance of the line, a transition will reflect back and forth along the line several times, and its amplitude at the receiving end will progressively approach its final value in staircase fashion as shown in Fig.A1. The degree of mismatch between the driver output impedance/receiver input impedance and the characteristic impedance of the line determines the amplitude and number of staircase steps. This phenomenon limits the transmission speed because it introduces a delay before the amplitude of the received transition falls below the specified maximum V_{IL} for a H/L transition, or rises above the specified minimum V_{OH} of the receiver for a L/H transition.

Alternatively, if the input impedance of the line receiver is higher than that of the line, and the output impedance of the line driver at $(V_{OH} - V_{OL})/2$ is lower than that of the line, the amplitude of each reflection will alternately overshoot and undershoot its final value. The degree of mismatch between the driver output impedance/receiver input impedance and the characteristic impedance of the line determines the amplitude and duration of the ringing. As shown in Fig.A2, there may be a considerable delay before the amplitude of the received signal ceases to fall below $V_{IH\,min}$ or rise above $V_{IL\,max}$ of the receiver. Apart from introducing a delay and limiting the transmission speed, the ringing can also reduce the dynamic noise margin and cause erroneous switching.

For 74HCT outputs (standard and bus logic) with the minimum specified output current at 85 °C driving unterminated lines with a characteristic impedance of between 75 Ω and 150 Ω, the situation depicted in Fig.A1 occurs for L/H and H/L transitions. For 74HCT ICs with the maximum specified output current at 25 °C, the situation depicted in Fig.A2 occurs for L/H and H/L transitions.

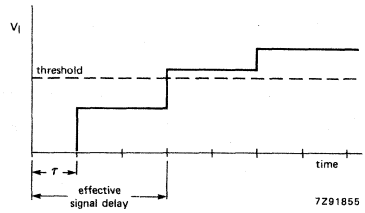


Fig.A1 A L/H transition at an unterminated receiver input when the output impedance of the driver is higher than that of the line

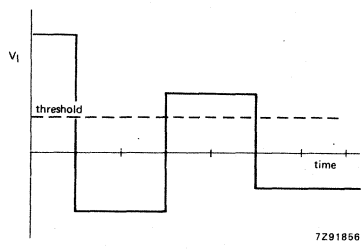


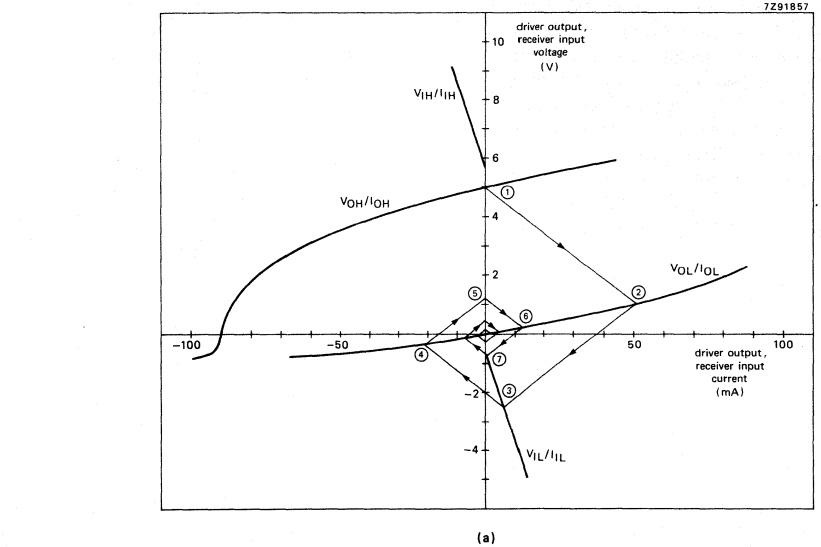
Fig.A2 A H/L transition at a receiver input when the output impedance of the driver is lower than that of the line

A Bergeron diagram can be used to determine the amplitude of the reflections at both ends of the transmission line. It shows the characteristic impedance of a transmission line as a series of load lines on the input and output characteristics of the line driver and receiver. The method of constructing it is to draw a load line for each input and output situation. Each load line originates from the previous quiescent point where the previous load line intersects the appropriate input/output characteristic. The slope of the load lines is equal to the characteristic impedance of the line but alternate load lines have opposite signs representing the change of current flow direction. The points where the load lines intersect the input/output characteristics indicate the amplitudes of the reflections.

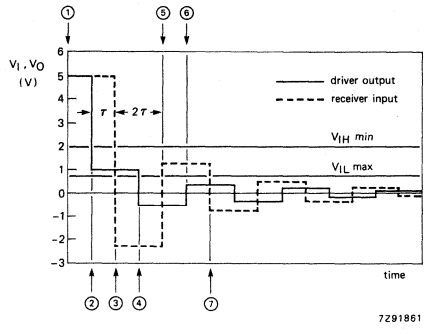
A Bergeron diagram for analysing reflections during a H/L transition from $V_{CC} = 5$ V to 0 V for a 74HCT bus driver is illustrated in Fig.A3. To ensure a worst-case calculation, a H/L transition is selected because the LOW noise margin is always less than the HIGH one. For the

same reason, the lowest practical transmission line impedance (75 Ω coaxial cable) is assumed and the 74HCT bus driver output characteristics in Fig.A3 represent the maximum output drive current. The input characteristic is the maximum input resistance when V_{IN} is within the limits of the supply rails. The input resistance when V_{IN} exceeds the limits of the supply rails is the ratio of input voltage to the current flow through the input polysilicon resistors and conducting diodes of the HCMOS input protection network. The resistance shown is maximum.

In Fig.A3, the first load line originates from the maximum HIGH level (5 V = point 1), has a slope of −1/75 Ω = −13,3 mA/V, and is extended to intersect the NMOS output characteristic at point 2. The next load line has a slope of +1/75 Ω and extends to intersect the input characteristic at point 3. This procedure continues, alternately intersecting the output and input characteristics until the 0 V/0 mA point is reached. Note that the effect of the input protection network on the input characteristic reduces the amplitude of the reflections from point 3 onwards. The voltage amplitudes at points 1 to 7 are plotted in Fig.A3(b) to show the effect of the ringing. It can be seen from Fig.A3(b) that the frequency of the ringing is ¼τ where τ is the propagation delay of the line. Propagation delays of various types of line and the associated ringing frequencies are given in Table A1.



(a)



(b)

Fig.A3 Bergeron diagram for a 74HCT bus driver transmitting a H/L transition along a 75 Ω line.
V_{CC} = 5 V, T_{amb} = 25 °C.
The currents are maximum

TABLE A1
Characteristics of transmission lines

type of line	Z_o (Ω)	τ(per m)	f_{ring}
stripline on 1,6 mm glass-epoxy pcb: 0,6 mm track over groundplane	120	7,2 ns	34,7 MHz/line length (m)
two 0,38 mm (28 SWG) pvc insulated wires twisted together	100	6,2 ns	40,3 MHz/line length (m)
coaxial cable RG-59B/U	75	5 ns	50 MHz/line length (m)

It can be seen from Fig.A3 that, if the line is terminated with its characteristic impedance at the receiving end, the line from point 2 will intersect a much lower impedance input characteristic and point 4 will be zero volts. In the interests of low quiescent power dissipation, it is desirable to use an a.c. termination consisting of a series RC network between the receiver input and ground as explained elsewhere in this article. All that remains is to calculate the value of the components for the RC network.

If a criterion of the frequency dependent component of the termination impedance being 20% of the total is assumed, the value of the resistor is $0{,}98\,Z_o$ and the value of the capacitor is:

$$C = \frac{1}{2\pi f_{ring} \times 0{,}2\,Z_o}$$

Using the values of f_{ring} and Z_o from Table A1 for a coaxial cable gives:

$$R = 75\,\Omega,\ C = 212\,pF \text{ per metre.}$$

Similarly, for a twisted pair:

$$R = 110\,\Omega,\ C = 180\,pF \text{ per metre.}$$

And for a stripline:

$$R = 120\,\Omega,\ C = 190\,pF \text{ per metre.}$$

An interesting feature of the a.c. termination is that, if it is used on a 3-state bus, it will maintain the bus at the last existing logic state if the bus goes to the high-impedance state for a short period (<100 μs).

To allow worst-case and best-case Bergeron diagrams to be constructed for all types of HCMOS logic elements, the maximum output current characteristics for 74HCT standard logic are shown in Fig.A4. The minimum output current characteristics for standard and bus driver 74HCT logic are shown in Fig.2.

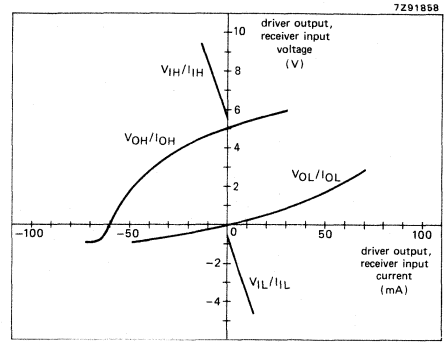
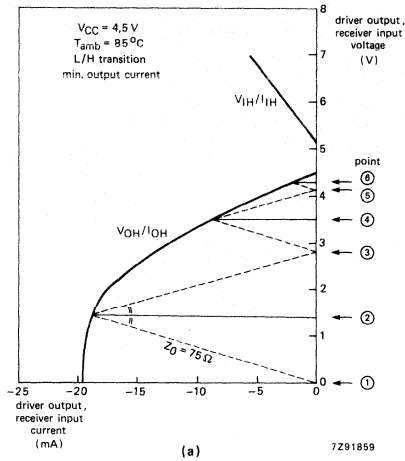


Fig.A4 Maximum V/I characteristics for standard 74HCT logic. V_{CC} = 5 V, T_{amb} = 25 °C

For the sake of completeness, Fig.A5 is a Bergeron diagram for a L/H transition from a 74HCT bus driver with the minimum specified output current at 85 °C. This gives a practical illustration of the staircase effect shown in Fig.A1.



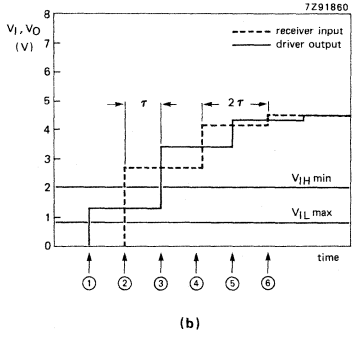


Fig.A5 Bergeron diagram for a 74HCT bus driver transmitting a L/H transition along a 75 Ω line. V_{CC} = 4,5 V, T_{amb} = 85 °C. The currents are minimum

MODIFYING LSTTL TEST PROGRAMS TO TEST HCMOS LOGIC ICs

For many years, LSTTL logic has been the established technology for interconnecting more complex VLSI circuits such as ALU, RAM and ROM. Consequently, circuit designers are familiar with it. However, the 74HC/HCT/HCU high-speed CMOS (HCMOS) family is establishing itself in the market as the natural successor to LSTTL in the role of interconnecting logic. Because of its low power dissipation and high speed, HCMOS is an alternative to LSTTL that drastically reduces power consumption without sacrificing system speed.

Furthermore, the LSTTL pin- and function-compatible 74HCT versions allow designers to replace LSTTL ICs in existing circuits. Interfacing with other logic families presents few problems as HCMOS is perhaps the most interface-flexible logic family available.

But the switch from LSTTL to HCMOS also makes it necessary for test personnel to change from testing LSTTL logic to the testing of HCMOS logic. This article outlines the basic criteria for converting test programs, takes an in-depth look at modifying the popular Teradyne J283 system for testing HCMOS, and briefly examines the possibilities of using other test systems.

WHY CONVERT?

If conversion of test programs from LSTTL to HCMOS involved replacing all test hardware and software, the high investment required could deter many potential users. But with the major test systems in use, replacement is not necessary. Converting test hardware and software involves minimal investment, of both capital and time.

The following test systems are in common use:

By manufacturers

- Teradyne J283 (particularly versions with both d.c. and functional test capabilities).
- Teradyne J325HV (used for CMOS testing, frequently by manufacturers who have never produced LSTTL).
- Manufacturers' custom-designed systems (Texas Instruments' LSTTL testers, and our CMOS systems, for example).
- MCT2000 tester (d.c. and a.c. parameters).

By users

- Gen Rad GR1732.
- Hewlett Packard HP5046.

(both widely used for incoming inspection).

The following characterization and qualification systems are used by both manufacturers and users:

- Sentry VII, Fairchild Series 20, and the GR16. These all have the flexibility needed for full functional/d.c. + a.c. evaluation. Auto-calibration routines improve "absolute accuracy" tests.

Conversion cost

As an introduction to converting test programs, conversion for the 74HC00 (quad 2-input NAND gate) will be sufficient to gain familiarity with the techniques involved, but it is only after a test conversion for, say an octal circuit, that a reliable estimate of the time required for converting all test programs can be made. The 8 buffer-outputs switching at one time will also reveal the a.c. response of the test-fixture and handler-interface. After establishing to what degree the test programs need to be altered, and the man-power available, a consistent and scheduled conversion strategy may considerably reduce the time needed for each circuit.

Assuming that a high-level programming language is to be used, the conversion time, compiling and hardware debugging should be no more than two to three man-hours per IC. Depending on how comprehensive your master program is, conditional compiling can also produce high and low temperature test programs at the same time.

COMPARING LSTTL AND HCMOS

Most modifications to the test programs result from the following fundamental differences between LSTTL and HCMOS:

- LSTTL is current-controlled whereas HCMOS is voltage-controlled.
- Static HCMOS gates have built-in redundancy. Either the p-channel pull-up transistor or the n-channel pull-down transistor is enough to perform the logic function. Test vectors applied in LSTTL testing, may therefore be inadequate to weed-out all open-circuit failures in HCMOS.

Open-circuit testing

As LSTTL ICs are current-controlled, truth-table testing will detect all short- and open-circuit faults, because internally charged nodes have insufficient residual charge to latch the preceding test vector. However, HCMOS ICs are voltage-controlled, so stored charge on internal nodes can be sufficient to latch the preceding state, thus the test programs could overlook open-source or open-drain connections to parallel p-channel (NAND) or n-channel (NOR) transistors.

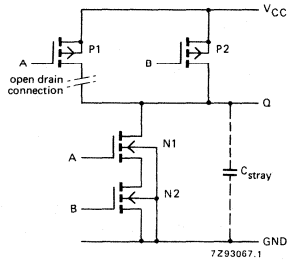


Fig.1 A basic NAND gate

To illustrate this, we will examine a basic NAND gate as shown in Fig.1. With inputs A and B both LOW, P_1 and P_2 conduct and output Q is HIGH. If input B is made HIGH, P_2 ceases to conduct but output Q remains HIGH as P_1 is still conducting. If, however, there was an open-circuit in the drain of P_1, output Q could still appear to be HIGH due to the stored charge on this circuit node.

It is therefore necessary to make output Q LOW (by making both inputs A and B HIGH) between these two test stages to guarantee that it is the action of P_1 that produces the HIGH output.

For this reason, truth-table testing must be extended. For the two-input NAND and NOR gates they become:

NAND GATE			NOR GATE		
inputs		output	inputs		output
A	B	Q	A	B	Q
0	0	1	0	0	1
[1	1	0]	0	1	0
0	1	1	[0	0	1]
[1	1	0]	1	0	0
1	0	1	[0	0	1]
1	1	0	1	1	0

[ ] indicates an additional line in the function table required for testing open-circuit drain or source connections.

As HCMOS ICs are voltage-controlled (energy-less), a similar problem occurs when detecting open feedback connections in flip-flops. Once the flip-flop is in the desired state, parasitic capacitances stay sufficiently charged to keep the flip-flop in that static state for several minutes, despite a missing feedback connection (to make it a static device). This situation is avoided by following this sequence:

1. At V_{CC} = 2 V, preset the IC.
2. Return logic inputs to LOW, leaving the output comparators of the tester connected.
3. Increase V_{CC} to 6 V.
4. If a flip-flop was non-static (due to open-circuit feedback), the outputs will now have flipped back to the opposite states; internal capacitances charged to 2 V (HIGH when V_{CC} = 2 V), will now be seen as LOW levels.
5. Repeat the sequence, but this time with opposite presets to the ICs.

Supply current

Although average system power consumption is lower for HCMOS than it is for LSTTL, testing of HCMOS imposes two new items:

Static mode test. HCMOS leakage current in any logic state should be low (in the region of nA). In LSTTL, a link has been found between faults in the IC and high I_{CC}. This is even more pronounced in HCMOS as excessive leakage current may load internal nodes, thus reducing the noise margins. Testing I_{CC} for every logic state combination takes a prohibitively long time (full A/D conversion), unless the test system has an analog comparison facility (for example, custom-built systems or as a special option on Teradyne J325HV). An acceptable solution is to test I_{CC} at enough logic states to ensure that all inputs and outputs have been both HIGH and LOW at least once each.

Dynamic behaviour during static mode testing. In LSTTL, switching from one logic state to the next does not produce high di/dt (current switched from one internal node to another is bearly detectable at the V_{CC} pin). In HCMOS however, heavy currents are drawn from V_{CC} during such transitions (several tens of mA because of the high di/dt from charging and discharging internal and external capacitances very rapidly). Therefore, an additional test for these transition currents is required. More stringent requirements are also placed on V_{CC} decoupling and chip capacitors close to the V_{CC} pin are necessary. This, however, is contradictory to the static mode test where parasitic leakage must be minimized. So, if relays are to be used to isolate the capacitors for the static mode test, they should be low-inductance reed relays.

Clock requirements

As long as the input drivers of the test system are able to drive inputs faster than 500 ns, there is no problem. Input rise and fall-times however, should be linear since a staircase shape can cause false triggering. Overshoots and ringing should be kept within 0,5 V of the supply rail voltage. All our 74HC/HCT ICs, however, are free from input and output induced latch-up so any overshoot will not lead to self destruction due to latch-up.

Input current

LSTTL has asymmetric characteristics, at both inputs and outputs. In the HIGH state, LSTTL has a rather high impedance, drawing leakage current in the order of only tens of μA. But in the LOW state, there is active current of several mA.

On the other hand, HCMOS inputs impose only a capacitive load, drawing a few nA in both HIGH and LOW states (tested at 6 V and 0 V respectively). This can give problems in low-temperature testing because a leakage current of a few microamps (due to the formation of condensation) can be ignored in LSTTL but not in HCMOS, which should only draw a few nA. Flushing the load-board and test socket with dry nitrogen overcomes this problem.

Output tests

Since in HCMOS, n- and p-channel transistors are laid-out to make them electrically identical, normal output load voltage tests can be applied with the following provisions:

- Force the current and measure the voltage. Otherwise, typical output currents at specified V_{OL} and V_{OH} may sometimes exceed the rated output currents.
- The output voltage HIGH for HCMOS is much higher than that for LSTTL. To obtain more accurate readings, a differential measurement between V_{CC} and the output should be made.

LSTTL CHARACTERISTICS THAT NEED NOT BE CHECKED FOR HCMOS

Output short-circuit current (I_{OS})

I_{OS} is not specified for HCMOS. Originally, I_{OS} was measured to reassure the TTL user that the circuit would withstand accidental output short-circuit to GND, and then in propagation delay calculation to define the ability of a circuit to charge the line capacitance. In HCMOS, however, there is no need to check I_{OS} because the purely capacitive loads allow extrapolation of a.c. parameters over the whole loading range.

DC input diode current (I_{IK})

As there are no Schottky-clamps on HCMOS inputs, it is unnecessary to check I_{IK}. ESD protection networks are integrated on-chip and inputs enter the circuit via a true (polysilicon) resistor. A test program should check only for diode-clamps (at a low current, about 100 μA, to eliminate the effect of the resistor from the measurement).

Note: specialized HCMOS ICs (HIGH-to-LOW logic converters) don't have an input protection diode connected to V_{CC}.

HCMOS CHARACTERISTICS THAT NEED SPECIAL TESTING

Noise margin

As HCMOS ICs are fast-switching and have high voltage gain between input and output, oscillation problems may be encountered (as with testing ALSTTL and FAST ICs). For ALSTTL and FAST, some manufacturers advise that noise margin tests should be omitted.

Since oscillation is an interaction between the IC characteristics and the hardware response of the test system, you should first try to improve the dynamic response of the supply to the device-under-test (DUT), by using ground-planes and high-frequency decoupling.

If the oscillation problem is still not solved, you can either skip the noise margin test or check the analog characteristic of the input stage. By measuring the I_{CC} current for 2 selected input voltages (see Fig.2), you can ensure that the noise margin specification is met, as follows:

1. Measure I_{CC} at specified V_{IL} (or V_{IH}).
2. Measure I_{CC} at specified $V_{IL} + 50$ mV (or $V_{IH} - 50$ mV); the current should be higher than during measurement 1.

Indirectly, you're sure to be on the correct side of the actual switching point of the input stage. The operation of subsequent stages, already at near full-swing (V_{CC} or GND) has already been checked by functional testing.

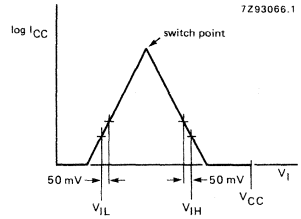


Fig.2 Measuring I_{CC} during noise margin test

V_{OL}/V_{OH} unloaded (20 μA load, 100 mV difference is allowed across the supply rails)

Having determined that the DUT is leakage-free for output HIGH and LOW, there is no need to perform unloaded output voltage tests, since the on-resistance of outputs is less than 100 Ω (0,4 V/4 mA min.). Even if all I_{CC} leakage was concentrated in one output stage, the total current drawn (160 μA for MSI + 20 μA external, for example) multiplied by R_{on} (<100 Ω) is 18 mV max., well within the 100 mV limit.

Resistance to latch-up

Good latch-up immunity can be obtained with a good lay-out (p^+-plugs closer to p-well than any n^+-diffusion) or by using epitaxial-wafers. These techniques have been combined to make HCMOS completely immune to latch-up.

Although bench testing (either d.c.-triggered or through-ramped V_{CC}-voltage tests) is likely to be more accurate for product characterization purposes, you can write an algorithm for your test system to compare the latch-up immunity of ICs from different manufacturers by following this procedure:

1. Supply the IC with 6 V. The power supply current clamp to be set to 200 mA.
2. Pulse (preferably 1 ms) the input or output under test with +10 mA (HIGH output) or −10 mA (LOW output).
3. Measure V_{CC}. If latch-up has occurred, the resulting hold-voltage will be much lower than 6 V.
4. Increase the pulse-current and go back to step 2.

For a comprehensive discussion on latch-up, see the section "Standardizing latch-up immunity tests".

AC characteristics

Experience in testing LSTTL, ALSTTL or FAST logic will have outlined the pitfalls which can be met when using test fixtures. Commercial load-boards and pin electronics are commonly laid-out as 50 Ω striplines, and while this is acceptable for ECL testing, and for simulating LSTTL resistive loads, with HCMOS it creates problems. Consider the following:

- HCMOS is specified with a 50 pF load. The lumped capacitance at the end of the stripline may not be seen by the IC output due to the substantial delay of the line compared to the transition time.
- Switching all 8 outputs of an octal IC simultaneously (each loaded with 50 pF), results in a massive load dump on the V_{CC} decoupling or groundplane, and ringing and overshoots are likely to occur. Switching outputs one at a time will relieve the problem.
- HCMOS reference levels are set at 50% of the transition. If reflection occurs in the system, the 50% point is right in the reflected area (see Fig.3). If you can't improve your test fixture, it might be more reliable to test at the 90% (t_{PHL}) or 10% (t_{PLH}) points. Correlated limits should be set to the specification value minus 50% of typical-specification transition times.

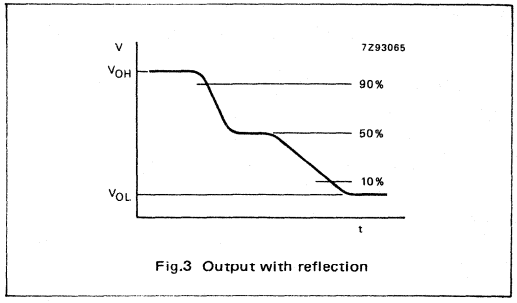


Fig.3 Output with reflection

- True "absolute accuracy" characterization calls for dedicated test fixtures. The more flexibility you build-in, the more concessions you have to make on accuracy.

TEST SYSTEM CONSIDERATIONS

Pin count (input only, output only, 3-state or multiplexed input/output)

For the HCMOS standard-range alone, a SSI/MSI tester may be adequate. More and more users, however, are changing to dedicated HCMOS ICs which integrate their system onto a single Gate- or Cell-Array chip. This secures copyright on the IC and gives a more reliable, simpler system. To match this trend, your test system should be able to handle configurations with more than 64 pins: even if this means partitioning the load-board into dedicated input and output pins.

Pin electronic (load-board) considerations

As detailed later under "Future options", a logarithmic scale for each I_{CC} test-vector may be valuable. Having loads connected to every output will substantially reduce the test duration.

Clock speed

For specialized ICs, maximum clock frequency testing may be necessary. Although abnormalities within the IC may often be revealed by I_{CC}/pattern testing, it could be necessary to test for full clock-frequency response in certain cases. As an option, MCT2000 gives you the opportunity to test 200 MHz functional response.

Pattern generation capability

For enhanced fault grading, software tools should be used to adapt the test vectors to HCMOS. Furthermore, the functional pattern your fault-grader generates must be easily downloadable into your test system.

Parametric measurement capability

– current range: 1 pA to 100 mA.

– voltage range: 10 mV to 30 V.

PROGRAMMING CONSIDERATIONS

High-level languages are recommended for HCMOS testing

Because input and output configurations are the same for every HCMOS IC, a high-level language (giving you the framework for the family through conditional compiling) is recommended. Together with the utility-programs already available in the "Master Operating Program", efficient data reduction may help you to grade different IC manufacturers and optimize the "fitness for use" in your application.

Throughput – reducing the test time

Depending on the preferences and prejudices of your manufacturers, you can skip certain parameter tests. PPM data (assuming full exchange of test information between user and manufacturer, avoiding test duplication) based on an open manufacturer-user relationship is helpful to optimize complete testing.

MODIFYING TERADYNE J283 TEST PROGRAMS FOR HCMOS

Modifying an existing LSTTL test program for the Teradyne J283 system is relatively straightforward. Following the guidelines previously given, adaptation of the patterns and parametric tests is possible. The level of fault-grading attainable is comparable with that for LSTTL testing.

The parameter tests that must be modified for use with HCMOS ICs can be divided into the following two categories:

1. Those tests that must be modified to obtain a "PASS" for HCMOS circuits. For these tests, it is only necessary to modify the settings that cause problems. This results in a test that confirms the ability of the HCMOS ICs to perform the LSTTL function.
2. Those tests that must be modified to test the IC to the HCMOS specification if the user wishes to take advantage of the additional features of HCMOS.

Category 1 tests

Input current at $V_I = 7$ V. Due to the input protection network of HCMOS ICs shown in Fig.4(b), input current will flow if the input voltage exceeds V_{CC} by 0,5 V or more. To prevent a "FAIL", the input voltage must be reduced from 7 V to V_{CC}. To test the exact input leakage current, the setting must be modified according to the d.c. characteristics for 74HCT circuits given in Appendix 2.

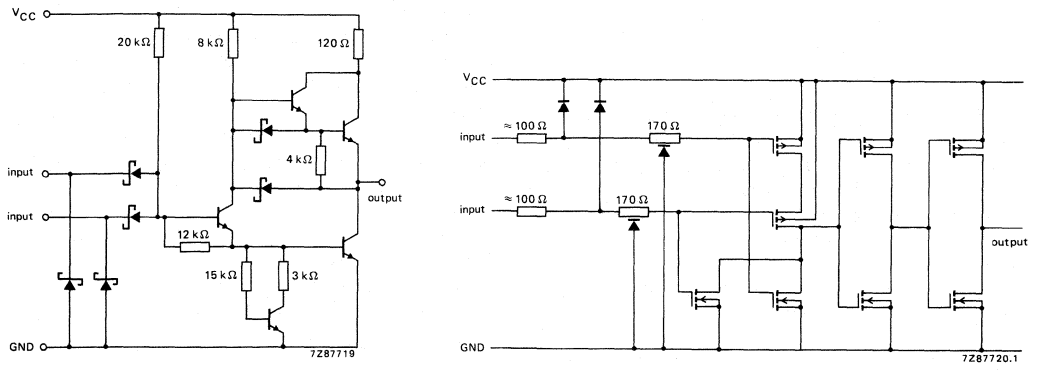


Fig.4 Comparison of LSTTL and HCMOS circuit structures.
(a) 2-input LSTTL NAND gate with totem-pole outputs (¼ 54/74LS00). For other structures, refer to published data;
(b) 2-input HCMOS NOR gate

Input clamp voltage. The protection network for each HCMOS IC input incorporates a series resistor that will cause the input clamp voltage with an input current of −18 mA to be much lower than the −1,5 V specified for LSTTL. Since the input clamp voltage is not specified for HCMOS circuits, this test could be omitted, or changed to have a conservative limit of −5 V. This assumes −3,6 V across a 200 Ω polysilicon input resistor plus −1,5 V across the input protection diode to GND.

Output short-circuit current HIGH. As shown in Appendix 1, LSTTL has an output short-circuit current (I_{OS}) of −20 mA to −100 mA. However, due to the symmetrical output structure of HCMOS ICs as shown in Fig.4(b), the LSTTL collector output resistor is not present. Since I_{OS} is not specified for HCMOS ICs, this test may be omitted.

Hysteresis (bus driver ICs). Many LSTTL bus driver ICs undergo a test for hysteresis using a 0,2 V minimum limit. HCMOS bus drivers don't have input hysteresis, so this test may be omitted, or the minimum hysteresis limit changed to 0 V.

Output voltage LOW at I_O = 12 mA (bus drivers types). Many LSTTL bus drivers have two specifications for V_{OL} test current that must be altered as shown below for HCMOS:

LSTTL		HCMOS	
$V_{OL\,max}$	I_{OL}	$V_{OL\,max}$	I_{OL}
0,4 V	12 mA	0,33 V	6 mA
0,5 V	24 mA	0,5 V	9 mA

These figures seem to indicate that the HCMOS LOW-level output current is less than that of LSTTL. The output t_{THL} of HCMOS however is similar to that of LSTTL. The real significance of the I_{OL} = 24 mA for LSTTL is the ability of its bus drivers to drive a d.c. terminated bus (see Fig.5(a)). However, this output current causes power dissipation of 250 mW per output (2 W per octal IC). For much lower power dissipation with an HCMOS IC, an a.c. termination as shown in Fig.5(b) is used.

Continuity. With some settings used for continuity testing, the input protection polysilicon resistor of HCMOS ICs could cause a "FAIL". This must be borne in mind when test engineers select their individual settings for this test. Therefore, it is important to keep input current to ±20 mA during continuity testing. With this current, the test voltage is ±5,5 V maximum.

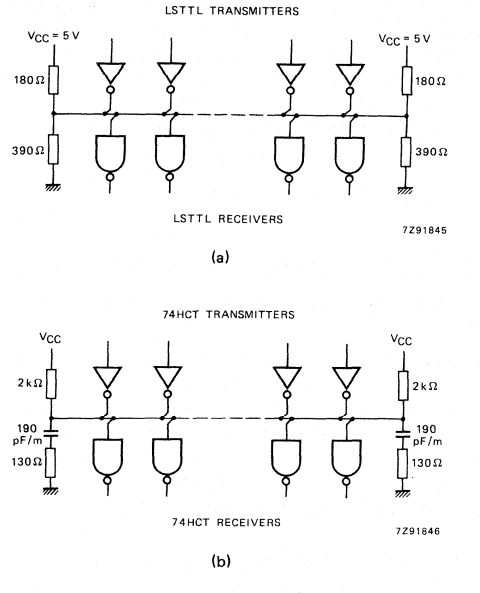


Fig.5 Termination of a 120 Ω stripline bus
(a) d.c. termination for LSTTL
(b) low-power a.c. termination for HCMOS

Category 2 tests

Quiescent supply current. Setting supply current I_{CC} for the output LOW condition for HCMOS ICs will not cause problems, but setting the output HIGH condition is more complex. In the Teradyne J283, there is a comparator connected to each of the outputs under test. These comparators cause an extra load current of about 7 μA per output, the precise current depending on the specific tester. The extra load currents are negligible compared with the I_{CC} of LSTTL ICs and can be ignored. When testing HCMOS circuits however, they can be very significant in comparison with the total I_{CC} and must be taken into account. A solution to this problem is to connect the HIGH outputs to V_{CC} so that they are excluded from the I_{CC} measuring path. This can be done with the statement:

MTEST V_{CC1} A B C (A, B, C are HIGH outputs in this test).

Output voltage LOW. The lower output voltages of HCMOS can be tested without any complications (4 mA for standard outputs, 6 mA for bus driver outputs).

Output voltage HIGH. The higher output voltages of HCMOS can be tested without any complications.

High impedance (OFF-state) output current for types having three-state outputs with $V_O = V_{CC}$ or GND. The high-impedance (OFF-state) leakage current (I_{OZ}) for HCMOS ICs can be tested without any complications, but with much tighter limits, as follows:

	LSTTL	HCMOS
I_{OZ}	20 μA	5 μA

Input leakage current (all HCMOS types). Input leakage current LSTTL tests can be run for HCMOS, but with much tighter limits, as follows:

	LSTTL	HCMOS
I_{IL}	−400 or −800 μA	−1 μA
I_{IH}	+20 or +40 μA	+1 μA

Function testing. This test can remain relatively unchanged because HCMOS and LSTTL ICs with the same type numbers have identical truth-tables. However, the requirement discussed for detecting open-drain or open-source connections (see "Comparing LSTTL and HCMOS – Open-circuit testing") must be met, and truth-table function tests modified accordingly.

USING OTHER TEST SYSTEMS FOR HCMOS

With the Teradyne J325HV, program changes are straightforward. The VDIF feature can be fully exploited to test for V_{OL}/V_{OH} loaded (as well as unloaded; see also "Supply current – Static mode test").

Our MCT2000 was originally set-up to test propagation delays and transition times. Practical experience however, has shown that it is suitable for a full data sheet check of d.c. parameters and function. As with the J283, output comparators cannot be fully isolated from the output-pins (solid-state switched, μA leakages are reported) and instead of I_{CC}, the leakage has to be measured in the GND line if one or more outputs are HIGH.

Another way of minimizing the leakage current drawn by the output comparators, is to set them in parametric mode and program the forced current to 0 nA.

The auto-calibration library contains the leakage current value per pin-card, and programming the current to zero will compensate for the remaining leakage current down to tens of nA.

For incoming inspection testing using the GR1732 or HP5045, in addition to existing machine limitations (e.g. inability to test for low leakages), care should be taken to ensure that the load board or its pin electronics don't influence the a.c. performance of the device under test.

Improving tester hardware/software for HCMOS testing

Teradyne's TTL testers are less appropriate for testing long counters (e.g. 2^{14} for 74HC/HCT4020 and 74HC/HCT4060, or 2^{12} for 74HC/HCT4040). While compiling the symbolic language into machine code, at least two computer words ($2 \times 10\,\mu s$) will be sent out and therefore $2^{14} \times 20\,\mu s = 330$ ms are needed for one functional pass. If you wire your clock input to the "word-one" pin cards, you can bypass the compiler by directly programming the "W1" in machine code, and since "W2" stays the same, you can halve the time for a functional pass.

On the J325, there is also the "burst" option which allows you to send out a high-speed burst of clock pulses in one functional pattern. During the burst, it is impossible to check the IC response but the logic state can be verified after the burst. Another helpful option on the J325 is the "I_{CC}-test per functional pattern". The buffered analog output of either VTEST (current monitor in V_{CC}) or MTEST (device supply from the parametric measurement unit PMU) is now connected to a square channel-card and can be monitored during each test vector with the digital comparators already built-in.

Future options

A logarithmic scale (as available on our custom-built testers) has proved to be essential for I_{CC} testing. Within a batch to be tested, I_{CC} ranges from pA to μA so, scale-compression at the high end (μA range) is required.

System specifications should be extended "up to and including" the handler-connectors. This requires interface standardization but it means that manufacturers and users will be working to the same standard. Currently, only MCT can comply with this requirement (being able to supply both tester and handler).

APPENDIX 1 DC characteristics for LSTTL circuits

These figures are for positive NAND gates and inverters with totem-pole outputs.
For the characteristics of other types, refer to published data for LSTTL circuits.

Voltage are referenced to GND (ground = 0 V)

			54LS			74LS				
parameter	V_{CC}	symbol	min.	typ.	max.	min.	typ.	max.	unit	conditions
Operating temperature	*	T_{amb}	−55	–	+125	0	–	+70	°C	
HIGH level input voltage	*	V_{IH}	2	–	–	2	–	–	V	
LOW level input voltage	*	V_{IL}	–	–	0,7	–	–	0,8	V	
Input clamp voltage	min.	V_{IK}	–	–	−1,5	–	–	−1,5	V	I_I = −18 mA
HIGH level output voltage	min.	V_{OH}	2,5	3,4	–	2,7	3,4	–	V	V_{IL} = max., I_{OH} = −400 μA
LOW level output voltage	min.	V_{OL}	–	–	–	–	0,25	0,4	V	V_{IH} = 2 V, I_{OL} = 4 mA
LOW level output voltage	min.	V_{OL}	–	0,25	0,4	–	0,35	0,5	V	V_{IH} = 2 V, I_{OL} = max.
Input current at V_I = 7 V	max.	I_I	–	–	0,1	–	–	0,1	mA	
HIGH level input current	max.	I_{IH}	–	–	20	–	–	20	μA	V_{IH} = 2,7 V
LOW level input current	max.	I_{IL}	–	–	−0,4	–	–	−0,4	mA	V_{IL} = 0,4 V
Short-circuit output current	max.	I_{OS}	−20	–	−100	−20	–	−100	mA	

For 54 LS, V_{CC} = 4,5 V to 5,5 V; for 74LS, V_{CC} = 4,75 V to 5,25 V.
All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
For short-circuit output current, only one output must be shorted, and for not more than one second.

* over V_{CC} range.

APPENDIX 2 DC characteristics for the 74HCT circuits

Voltages are referenced to GND (ground = 0 V)

parameter	V_{CC} (V)	symbol	T_{amb} (°C)							unit	conditions	
			+25			−40 to +85		−40 to +125			V_I	others
			min	typ	max	min	max	min	max			
HIGH level input voltage	4,5 to 5,5	V_{IH}	2,0	1,6	–	2,0	–	2,0	–	V		
LOW level input voltage	4,5 to 5,5	V_{IL}	–	1,2	0,8	–	0,8	–	0,8	V		
HIGH level output voltage all outputs	4,5	V_{OH}	4,4	4,5	–	4,4	–	4,4	–	V	V_{IH} or V_{IL}	$-I_O = 20\,\mu A$
HIGH level output voltage standard outputs	4,5	V_{OH}	3,98	4,32	–	3,84	–	3,7	–	V	V_{IH} or V_{IL}	$-I_O = 4,0$ mA
HIGH level output voltage bus driver outputs	4,5	V_{OH}	3,98	4,32	–	3,84	–	3,7	–	V	V_{IH} or V_{IL}	$-I_O = 6,0$ mA
LOW level output voltage all outputs	4,5	V_{OL}	–	0	0,1	–	0,1	–	0,1	V	V_{IH} or V_{IL}	$I_O = 20\,\mu A$
LOW level output voltage standard outputs	4,5	V_{OL}	–	0,15	0,26	–	0,33	–	0,4	V	V_{IH} or V_{IL}	$I_O = 4,0$ mA
LOW level output voltage bus driver outputs	4,5	V_{OL}	–	0,16	0,26	–	0,33	–	0,4	V	V_{IH} or V_{IL}	$I_O = 6,0$ mA
Input leakage current	5,5	$\pm I_I$	–	–	0,1	–	1,0	–	1,0	μA	V_{CC} or GND	
3-state output OFF-state current	5,5	$\pm I_{OZ}$	–	–	0,5	–	5,0	–	10,0	μA	V_{IH} or V_{IL}	*
Quiescent supply current												
SSI	5,5	I_{CC}	–	–	2,0	–	20,0	–	40,0	μA	V_{CC}	$I_O = 0$
flip-flops	5,5	I_{CC}	–	–	4,0	–	40,0	–	80,0	μA	or	$I_O = 0$
MSI	5,5	I_{CC}	–	–	8,0	–	80,0	–	160,0	μA	GND	$I_O = 0$

* $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$.

HANDLING PRECAUTIONS

Electrostatic charges

Electrostatic charges can be stored in many things; for example, man-made fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depends on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our CMOS ICs are internally protected against electrostatic discharge, but they can be damaged if the following precautions are not taken.

Work station

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is 1 kΩ to 0,5 MΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work-bench should be earthed via a wrist strap and a resistor.
- All electrical equipment should be connected to the mains via an earth-leakage switch and the equipment cases should be earthed.
- Relative humidity should be maintained between 50% and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

CMOS ICs are packed for despatch in antistatic/conductive boxes, rails or blister tape. The fact that the ICs are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The ICs should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the task should be performed at a protected work station. Any CMOS ICs that are temporarily stored should be packed in conductive or antistatic packing or carriers.

Assembly

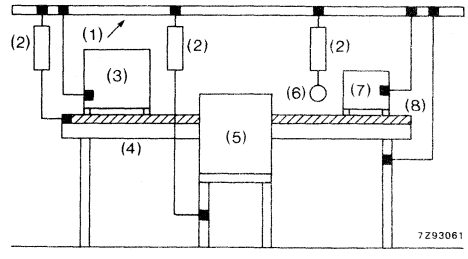
CMOS ICs must be removed from their protective packing with earthed component-pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Don't remove more ICs from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the CMOS ICs are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand-tools should be of conductive or antistatic material and, where possible, not insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board doesn't touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Handle assembled circuit boards containing CMOS ICs in the same way as unmounted CMOS ICs. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail
(2) Resistor (500 kΩ ± 10%, 0,5 W)
(3) Ionizer
(4) Work bench
(5) Chair
(6) Wrist strap
(7) Electrical equipment
(8) Conductive surface/ antistatic sheet

Fig. 1 Protected work station.

QUALITY INFORMATION

QUALITY – HCMOS LOGIC ICs

QUALITY ASSURANCE

Our Quality Department is fully involved in all stages of the production cycle of our HCMOS family of logic ICs:

- design and development
- wafer fabrication
- assembly
- inspection and testing
- batch release
- customer liaison.

This results in continuous feedback of data which enables us to refine production conditions, test methods and designs to yield optimum quality in the final application.

Design and development

Layout rules and design parameters for our HCMOS family of ICs are specified in our Design Manual which reflects more than ten years' experience in CMOS silicon-gate production.

During the CAD generation of new circuit designs, layouts are automatically checked against the rules laid down in the Design Manual. Each layout is further checked by the Quality Department against not only the Design Manual requirements, but also the capabilities of the assembly process and product specifications.

Wafer fabrication

To realize the full performance potential of our HCMOS technology we have developed a new organizational structure for the wafer fabrication process. Production flow is now divided between technology-oriented Control Groups that are responsible for

- process control
- equipment engineering
- calibration
- contamination control
- training.

Activities of these Groups are coordinated by Process Engineering and supported by extensive data-processing facilities.

Figure 1 shows the flow of wafers through the various fabrications stages and the associated process controls. Overall wafer fabrication activity, Fig.2, is monitored by frequent audits by the Quality Department.

Assembly

Quality control is fully integrated with the assembly process, as shown in Fig.3.

Dice are assembled into packages on highly automated assembly lines. Fully automatic die attach and wire bonding ensure a high and consistent assembly quality. Tube to tube handling after moulding ensures excellent mechanical and visual quality.

Quality improvement programme

To develop quality awareness in all areas of our Integrated Circuit Group, we have instituted a 14-step Quality Improvement Programme. This programme, with its regular Quality College courses, is designed to improve all aspects of our IC-business by:

- Monitoring the quality of
  - R&D
  - wafer fabrication
  - assembly
  - marketing and sales
  - support services
  - stores and shipping.
- Extending responsibility for error-cause removal to everyone in the operation.
- Making everyone aware of performance indicators.
- Improving response to customers' problems and improving resultant cause tracing.
- Continuous analysis of product performance to enable continual specification improvement.
- Regular quality audits and analysis.

We are totally committed to quality improvement and invite our customers to share in achieving it.

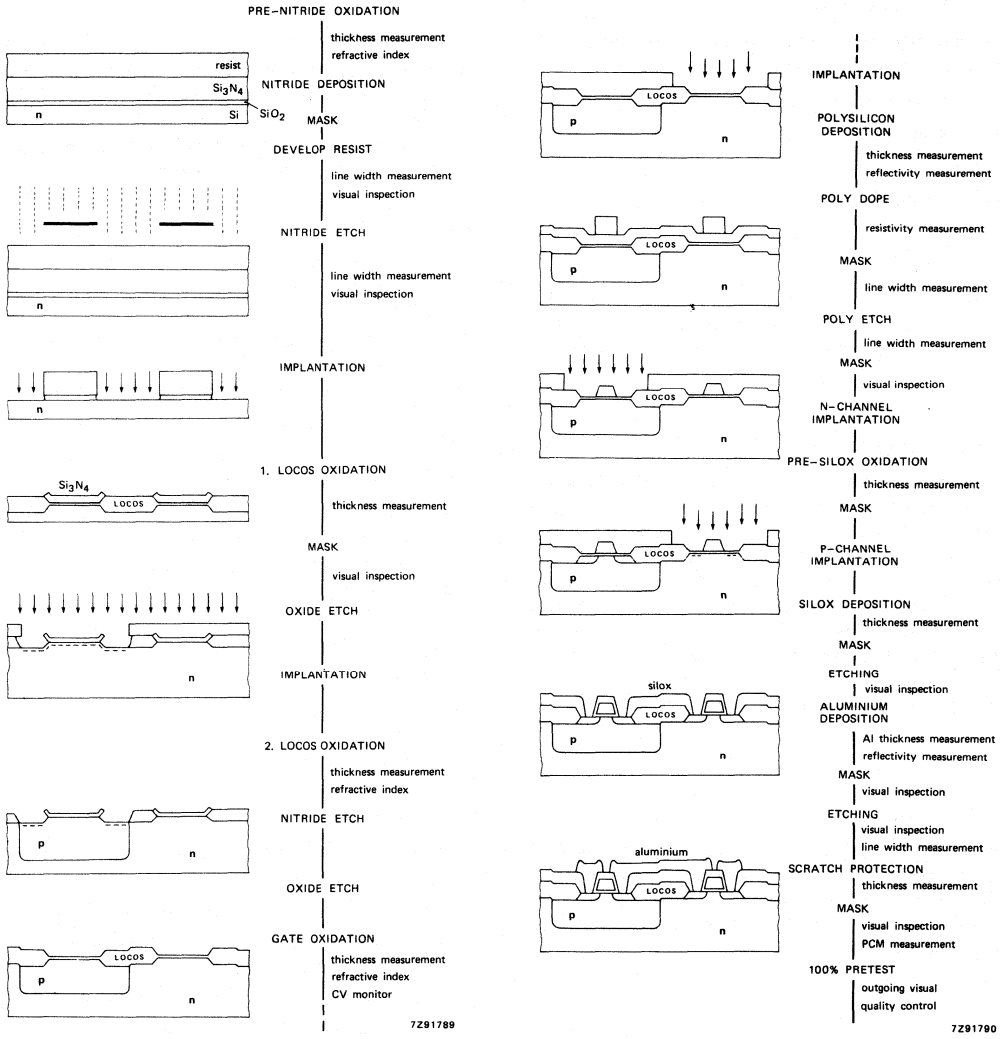


Fig.1 Wafer fabrication flow chart for our HCMOS ICs

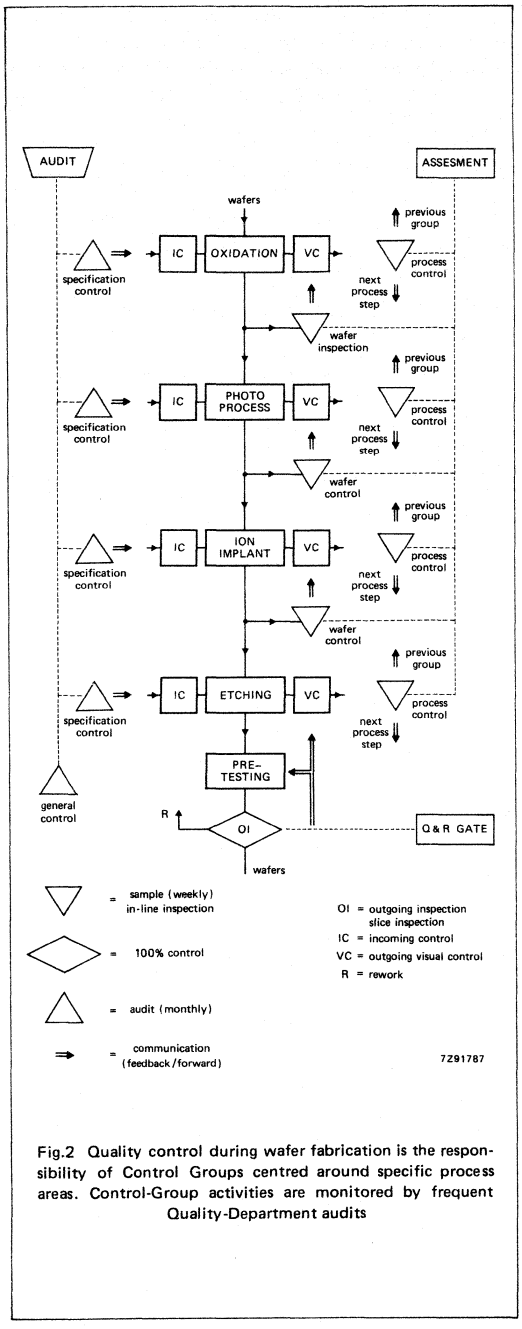


Fig.2 Quality control during wafer fabrication is the responsibility of Control Groups centred around specific process areas. Control-Group activities are monitored by frequent Quality-Department audits

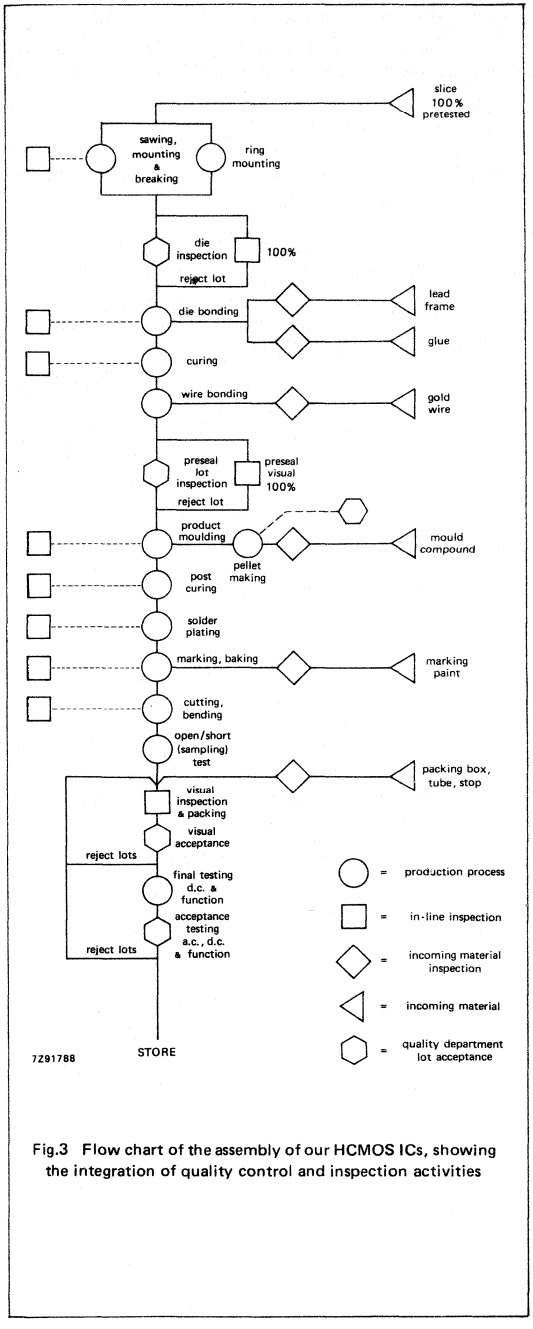


Fig.3 Flow chart of the assembly of our HCMOS ICs, showing the integration of quality control and inspection activities

NEW PRODUCT RELEASE

The Quality Department is involved not only in the design and development phases of new products, but also in the qualification and approval of new diffusion processes, packages and assembly methods. Improvements or changes in either product or process must be fully specified, qualified and approved before entering production. As an example, Table 1 lists the qualification tests for a new wafer fabrication process.

TABLE 1
Wafer fabrication process qualification tests

test	conditions	duration
electrical endurance	150 °C, 6 V	2000 h
electrical endurance	175 °C, 6 V	2000 h
THB	85 °C, 85% RH, 6 V	2000 h
autoclave	132 °C, 85% RH, 6 V	150 h
temperature cycling	−65 °C to 150 °C	1000 cycl.
storage — low temperature	−65 °C	1000 h
storage — high temperature	+150 °C	1000 h
electrostatic discharge	1,5 kΩ, 100 pF, >2 kV	—

ACCEPTANCE AND PERIODIC TESTING

Following the 100% final electrical test, each lot of our HCMOS ICs is sampled by the Quality Department for Acceptance testing. In Group A, a full inspection over the rated temperature range is performed on each device to the following AQLs:

	AQL (combined) (%)	inspection level
functional + electrical parameters	0,1	II
visual + mechanical	0,1	II

Electrical parameters include all those quoted in the device Data Sheet; visual and mechanical inspection includes marking legibility, straightness of pins, plating and appearance.

A further sample is drawn weekly from each structurally-similar group of ICs and subjected to Group B testing:

- dimensions
- solderability
- temperature cycling (10 cycles)
- electrical endurance (168 h at 125 °C).

To explore quality in further depth, each structurally-similar group is further sampled quarterly and subjected to Group C Tests (see Table 8). Some THB tests and endurance tests of longer than 1000 h are also performed to examine long-term effects.

Every reject, found by us or returned by a customer, is subjected to in-depth failure analysis using the most comprehensive and up-to-date equipment. The results obtained provide valuable data that is used for continual product improvement.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

The improved CMOS technology used for our HCMOS family allows polysilicon resistors to be used at all inputs to slow down fast input transients due to electrostatic discharges and dissipate some of their energy. Despite the improved protection provided by these resistors, and the use of two stages of diode clamping, Fig.4, the usual CMOS handling precautions should still be observed. (See the section Handling Precautions.)

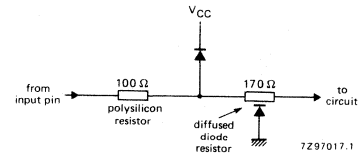


Fig.4 Input network used to protect our HCMOS ICs from electrostatic discharge

ESD resistance of our HCMOS is measured for both positive and negative discharge from a 100 pF capacitor through a 1,5 kΩ resistor. Pulse rise time is 13±2 ns. Results obtained from Acceptance testing are given in Table 2.

TABLE 2
ESD resistance of our HCMOS ICs (cumulative results)

	polarity	1% fail	50% fail
inputs	positive	2050 V	2700 V
	negative	2300 V	>3000 V
outputs		>3000 V	>3000 V
supply		>3000 V	>3000 V

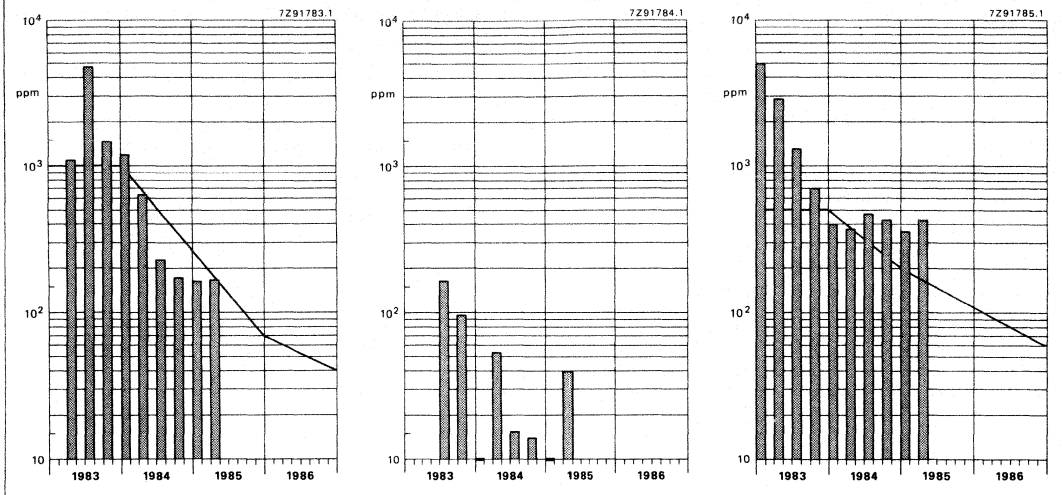


Fig.5 Process average rejects level (in ppm) for (a) electrical parameters and functions combined; (b) function only; (c) mechanical and visual defects. Target quality levels are also indicated

OUTGOING QUALITY

The results from Quality Department Acceptance testing provide a good indication of the outgoing quality of our HCMOS ICs. Figure 5 shows, in terms of 'electrical parameters and functions' and 'mechanical and visual', the reject levels recorded in ppm (parts per million) for 1983, 1984 and the first half of 1985, together with the projected levels for 1985 and 1986.

ENDURANCE AND ENVIRONMENTAL TEST RESULTS

Temperature-humidity-bias

THB testing measures the moisture resistance of plastic DIL and SO packages. It is performed at 85 °C and 85% relative humidity with V_{CC} = 6 V. Electrical measurements (against the Device Specification) are made after 168 h, 500 h, 1000 h and every 1000 h thereafter. Functional failures are subjected to failure analysis.

Results from tests done from 1983 to September 1985, Table 3, show the excellent moisture resistance of our packages, even after extended test durations.

Results of THB testing confirm that there is no significant difference between the results of tests on ICs in DIL and SO packages.

TABLE 3
Temperature-humidity-bias (85 °C/85% RH/6 V)

DIL package

test time (h)	sample N	failures (cum) param.	failures (cum) function	cumulative % failure
1000	1685	3	3	0,36
2000	1018	3	6	0,88
3000	420	5	8	3,10
4000	360	6	5	3,06
6000	120	3	3	5,00

SO package

test time (h)	sample N	failure (cum) param.	failure (cum) function	cumulative % failure
1000	350	0	0	0
2000	100	0	0	0
3000	40	0	0	0

Failure analysis of rejects:
Parameter: I_{CC} leakage.
Function: mostly corrosion, some I_{CC} leakage.

Autoclave with bias

This is essentially an accelerated THB test with an acceleration factor of 30. This means that 120 hours' autoclave is comparable with 3600 hours' THB. We have extended the conventional autoclave test to include 6 V bias at a temperature of 132 °C in unsaturated steam at a relative humidity of 85% and a pressure of 250 kPa (2,5 atmospheres). The results given in Table 4 attest to the excellence of the silicon-nitride/polysilicon-gate protection layer and the workmanship of the package.

TABLE 4
Autoclave with bias (132 °C/85% RH/6 V)

DIL package

test time (h)	sample N	failures (cum) param.	failures (cum) function	cumulative % failure
120	700	6	3	1,29
180	530	1	6	1,32
240	530	5	13	3,40
300	530	3	23	4,91
360	480	3	31	7,08

SO package

test time (h)	sample N	failures (cum) param.	failures (cum) function	cumulative % failure
120	355	5	3	2,25
180	210	0	3	1,43
240	150	0	2	1,33
300	150	0	2	1,33
360	60	0	0	0

Failure analysis of rejects:
Parameter: I_{CC} leakage.
Function: mostly corrosion, some I_{CC} leakage.

Accelerated life testing

To obtain data for failure rate predictions quickly, some life tests are done at raised temperatures. ICs are powered by their maximum supply voltage; ambient temperatures are up to 150 °C for ICs in plastic packages, and 225 °C for ICs in special/ceramic evaluation packages. ICs are tested for function and electrical parameters before the test starts, and then after 48 h, 168 h, 1000 h, and then every 1000 h. Every failure found is analysed. The results from such testing of many types of 74HC and 74HCT ICs in plastic DIL and SO packages are summarized in Tables 5 and 6. No significant difference between te results obtained from different packages has been detected. In Table 6 the results given in Table 5 are derated to 50 °C operating temperature, using an activation energy E_A of 0,7 eV. Figure 6 gives the derate failure rates for various activation energies.

TABLE 5
Life test results: HCMOS, 1983/Sept. '85 (cumulative)

T (°C)	test duration (h) 1000	2000	4000	8000
	(failures/sample)			
Plastic DIL				
125	0/77			
150	9/3600	8/1289	2/568	2/160
175	2/320	3/320	3/80	
225	0/48			
6 x parameter (I_{CC}), 6 x function (I_{CC}, gate oxide)				
SO				
150	2/692	1/176	1/80	1/40
1 x parameter (I_{CC}), 1 x function (gate oxide)				

TABLE 6
Failure rates (from test data of Table 5)

test temp. T (°C)	device hours (10^6)	50 °C device hours (10^6)	failures
Plastic DIL			
125	0,077	8,8	0
150	6,465	2463,1	9
175	0,800	892,6	3
225	0,048	330,7	0
	Total:	3695,2	12
SO			
150	1,188	452	2

Extrapolated failure rate at 50 °C for E_A = 0,7 eV

Plastic DIL: λ = 3,2 FITS (3,2 x 10^{-9}/h);
λ = 4,3 FITS (4,3 x 10^{-9}/h) at 60% confidence
SO: λ = 4,4 FITS (4,4 x 10^{-9}/h);
λ = 6,8 FITS (6,8 x 10^{-9}/h) at 60% confidence

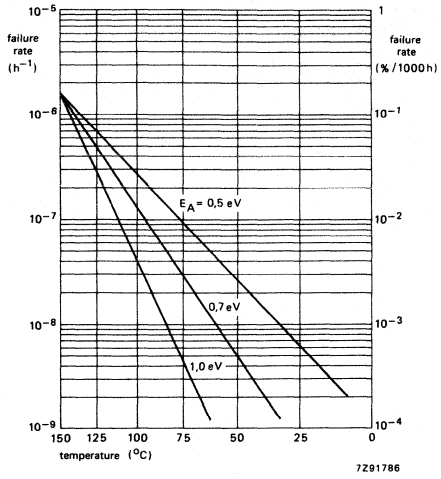


Fig.6 Projected failure rates for our HCMOS ICs as a function of temperature, with activation energy as parameter

Temperature cycling

Cycling between −65 °C and +150 °C generates stresses that test the structural integrity of dice and packages. We perform this test according to the requirements of MIL-STD-883C, Method 1010, Condition C. Samples are checked before and after the test for function and electrical parameters against the published values. Two failures have been observed in 1200 cycles, as reported in Table 7.

TABLE 7
Temperature cycling: −65 °C to +150 °C in dry air

	DIL		SO	
no. of cycles	samples	failures (cum)	samples	failures (cum)
200	1686	0	1016	0
400	1492	0	1016	0
800	997	0	1016	1
1200	360	0	594	2
1600	195	0	288	0
2000	195	0	288	
2400	195	0		

failures: 2 x die crack.

RELIABILITY TEST PROGRAM

Conditions for the endurance tests performed regularly on structurally-similar groups of our HCMOS products are derived from IEC68 and MIL-STD-883C specifications. These are listed in Table 8, together with results obtained during 1983 and 1984.

CECC RELEASE

The CECC (CENELEC Electronic Components Committee) Quality System, which dates from the early 1970s, harmonizes quality standards throughout Europe; fifteen countries now participate. Electronic components released under CECC must have satisfied the inspection requirements of the appropriate CECC Specification. The inspection and the application of the CECC System by suppliers are monitored by independent National Supervising Inspectorates, such as the British Standards Institute in the UK.

The component specification, which describes the component in sufficient detail to enable a customer to select it for a particular application, includes

- electrical values and their tolerances and limits
- behaviour under defined climatic, mechanical and endurance conditions
- acceptance criteria for batches of the component.

To qualify for the CECC Mark or Certificate of Conformity

a component manufacturer must satisfy the National Supervising Inspectorate that:

- his Quality Department runs strictly according to CECC rules, and especially that it is independent of Production Management
- his production departments run according to CECC rules for each component inspected.

Our HCMOS products received official CECC approval in the second half of 1985.

TABLE 8
Periodic reliability test program: 1983/1984 results

sub-group	description	IEC 68	derived from MIL-STD-883C method no.	plastic DIL N	plastic DIL n_F	SO N	SO n_F
C1	dimensions	–	2016	324	0	36	0
C2	marking permanence	–	2015	440	0	72	0
C3	robustness of termination	68-2-21	2004	234	0	108	0
	– tensile	Test Ua	cond. A				
	– bending	Test Ub	cond. B1				
	– lead fatigue	Test Ub	cond. B2				
C4	temperature treatments (sequential)			1739	0	157	0
	– resistance to soldering heat (10 s at 300 °C)						
	– thermal shock (10 x 0 °C to 100 °C)	68-2-27 Test Nc	1011 cond. A				
	– temperature cycling (10 x –65 °C to +150 °C)	68-2-14 Test Na	1011 cond. C				
	– storage to 85 °C and 85% RH for 21 days						
C6	THB* 85 °C/85% RH/6 V/1000 h	68-2-3 Test Ca	1004	(see Table 3)			
C8	electrical endurance 1000 h at 125 °C		1005	(see Tables 5 and 6)			
C10	temperature cycling						
	200 x –65 °C to +150 °C	68-2-14 Test B	1010 cond. C	1686	0	1016	0
C11	storage endurance	68-2-2 Test Ba	1008 cond. C	863	0	105	0
	1000 h at T_a = 150 °C						
C12	storage endurance	68-2-1 Test Ab		625	0	105	0
	1000 h at T_a = –65 °C						
C13	transient energy		3015				
C15	salt mist	68-2-11 Test Ka	1009 cond. A				
	solderability	68-2-20 Test T	2003	960	1	384	0
	autoclave						
	121 °C/100% RH/60 h			548	0	160	0

* Temperature-humidity-bias.

N = sample size.
n_F = number failures.

SELECTION GUIDE

HCMOS 74HC/HCT/HCU FAMILY

Type numbers have a suffix which signifies the type of package:
P = plastic DIL; T = plastic SO mini-pack

type no.	description	pins	classification
NAND/NOR gates/EXCLUSIVE-NOR gates			
HC/HCT00	quad 2-input NAND gate	14	SSI
HC/HCT02	quad 2-input NOR gate	14	SSI
HC/HCT03	quad 2-input NAND gate (with open drain outputs)	14	SSI
HC/HCT10	triple 3-input NAND gate	14	SSI
HC/HCT20	dual 4-input NAND gate	14	SSI
HC/HCT27	triple 3-input NOR gate	14	SSI
HC/HCT30	8-input NAND gate	14	SSI
HC7266	quad 2-input EXCLUSIVE-NOR gate	14	SSI
HC/HCT4002	dual 4-input NOR gate	14	SSI
AND/OR/EXCLUSIVE-OR gates			
HC/HCT08	quad 2-input AND gate	14	SSI
HC/HCT11	triple 3-input AND gate	14	SSI
HC/HCT21	dual 4-input AND gate	14	SSI
HC/HCT32	quad 2-input OR gate	14	SSI
HC58	dual AND-OR gate	14	SSI
HC/HCT86	quad 2-input EXCLUSIVE-OR gate	14	SSI
HC/HCT4075	triple 3-input OR gate	14	SSI
Inverters/buffers/line drivers/level shifters			
HC/HCT04	hex inverter	14	SSI
HCU04	hex inverter (unbuffered)	14	SSI
HC/HCT125*	quad buffer/line driver; 3-state; output enable active LOW	14	MSI
HC/HCT126*	quad buffer/line driver; 3-state; output enable active HIGH	14	MSI
HC/HCT240*	octal buffer/line driver; 3-state; inverting	20	MSI
HC/HCT241*	octal buffer/line driver; 3-state; output enable active LOW or HIGH	20	MSI
HC/HCT244*	octal buffer/line driver; 3-state; output enable active LOW	20	MSI
HC/HCT365*	hex buffer/line driver; 3-state	16	MSI
HC/HCT366*	hex buffer/line driver; 3-state; inverting	16	MSI
HC/HCT367*	hex buffer/line driver; 3-state	16	MSI
HC/HCT368*	hex buffer/line driver; 3-state; inverting	16	MSI
HC/HCT540*	octal buffer/line driver; 3-state; inverting	20	MSI
HC/HCT541*	octal buffer/line driver; 3-state	20	MSI
HC4049	hex inverting HIGH-to-LOW level shifter	16	SSI
HC4050	hex HIGH-to-LOW level shifter	16	SSI

* Types with a bus-driver output stage.

Type numbers have a suffix which signifies the type of package:
P = plastic DIL; T = plastic SO mini-pack

type no.	description	pins	classification
Flip-flops/latches/registers			
HC/HCT73	dual JK flip-flop with reset; negative-edge trigger; supply on centre pins	14	FF
HC/HCT74	dual D-type flip-flop with set and reset; positive-edge trigger	14	FF
HC/HCT75	quad bistable transparent latch	16	FF
HC/HCT107	dual JK flip-flop with reset; negative-edge trigger	14	MSI
HC/HCT109	dual JK flip-flop with set and reset; positive-edge trigger	16	FF
HC/HCT112	dual JK flip-flop with set and reset; negative-edge trigger	16	FF
HC/HCT173*	quad D-type flip-flop; positive-edge trigger; 3-state	16	MSI
HC/HCT174	hex D-type flip-flop with reset; positive-edge trigger	16	MSI
HC/HCT175	quad D-type flip-flop with reset; positive-edge trigger	16	MSI
HC/HCT259	8-bit addressable latch	16	MSI
HC/HCT273	octal D-type flip-flop with reset; positive-edge trigger	20	MSI
HC/HCT373*	octal D-type transparent latch; 3-state	20	MSI
HC/HCT374*	octal D-type flip-flop; positive-edge trigger; 3-state	20	MSI
HC/HCT377	octal D-type flip-flop with data enable; positive-edge trigger	20	MSI
HC/HCT533*	octal D-type transparent latch; 3-state; inverting	20	MSI
HC/HCT534*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting	20	MSI
HC/HCT563*	octal D-type transparent latch; 3-state; inverting; bus oriented pin-out	20	MSI
HC/HCT564*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting; bus oriented pin-out	20	MSI
HC/HCT573*	octal D-type transparent latch; 3-state; bus oriented pin-out	20	MSI
HC/HCT574*	octal D-type flip-flop; positive-edge trigger; 3-state; bus oriented pin-out	20	MSI
HC/HCT670*	4 x 4 register file; 3-state	16	MSI
HC/HCT7030	9-bit x 64-word FIFO register; 3-state	28	MSI
HC/HCT40105	4-bit x 16-word FIFO register	16	MSI
Shift registers			
HC/HCT164	8-bit serial-in/parallel-out shift register	14	MSI
HC/HCT165	8-bit parallel-in/serial-out shift register	16	MSI
HC/HCT166	8-bit parallel-in/serial-out shift register; with reset	16	MSI
HC/HCT194	4-bit bidirectional universal shift register	16	MSI
HC/HCT195	4-bit parallel access shift register	16	MSI
HC/HCT299*	8-bit universal shift register; 3-state	20	MSI
HC/HCT597	8-bit shift register with input flip-flops	16	MSI
HC/HCT7597	8-bit shift register with input latches		
HC/HCT4015	dual 4-bit serial-in/parallel-out shift register	16	MSI
HC/HCT4094	8-stage shift-and-store bus register	16	MSI
HC/HCT40104*	4-bit bidirectional universal shift register; 3-state	16	MSI

* Types with a bus-driver output stage.

Type numbers have a suffix which signifies the type of package:
P = plastic DIL; T = plastic SO mini-pack

type no.	description	pins	classification
Arithmetic circuits			
HC/HCT85	4-bit magnitude comparator	16	MSI
HC/HCT181	4-bit arithmetic logic unit	24	MSI
HC/HCT182	look-ahead carry generator	16	MSI
HC/HCT280	9-bit odd/even parity generator/checker	14	MSI
HC/HCT283	4-bit binary full adder with fast carry	16	MSI
HC/HCT583	4-bit BCD full adder with fast carry	16	MSI
HC/HCT688	8-bit magnitude comparator	20	MSI
Counters			
HC/HCT93	4-bit binary ripple counter	14	MSI
HC/HCT160	presettable synchronous BCD decade counter; asynchronous reset	16	MSI
HC/HCT161	presettable synchronous 4-bit binary counter; asynchronous reset	16	MSI
HC/HCT162	presettable synchronous BCD decade counter; synchronous reset	16	MSI
HC/HCT163	presettable synchronous 4-bit binary counter; synchronous reset	16	MSI
HC/HCT190	presettable synchronous BCD decade up/down counter	16	MSI
HC/HCT191	presettable synchronous 4-bit binary up/down counter	16	MSI
HC/HCT192	presettable synchronous BCD decade up/down counter	16	MSI
HC/HCT193	presettable synchronous 4-bit binary up/down counter	16	MSI
HC/HCT390	dual decade ripple counter	16	MSI
HC/HCT393	dual 4-bit binary ripple counter	14	MSI
HC/HCT4017	Johnson decade counter with 10 decoded outputs	16	MSI
HC/HCT4020	14-stage binary ripple counter	16	MSI
HC/HCT4024	7-stage binary ripple counter	14	MSI
HC/HCT4040	12-stage binary ripple counter	16	MSI
HC/HCT4059	programmable divide-by-n counter	24	MSI
HC/HCT4060	14-stage binary ripple counter with oscillator	16	MSI
HC/HCT4510	BCD up/down counter	16	MSI
HC/HCT4516	binary up/down counter	16	MSI
HC/HCT4518	dual synchronous BCD counter	16	MSI
HC/HCT4520	dual synchronous 4-bit binary counter	16	MSI
HC/HCT40102	8-stage synchronous BCD down counter	16	MSI
HC/HCT40103	8-bit synchronous binary down counter	16	MSI
Multiplexers			
HC/HCT151	8-input multiplexer	16	MSI
HC/HCT153	dual 4-input multiplexer	16	MSI
HC/HCT157	quad 2-input multiplexer	16	MSI
HC/HCT158	quad 2-input multiplexer; inverting	16	MSI
HC/HCT251	8-input multiplexer; 3-state	16	MSI

* Types with a bus-driver output stage.

Type numbers have a suffix which signifies the type of package:
P = plastic DIL; T = plastic SO mini-pack

type no.	description	pins	classification
Multiplexers (continued)			
HCT/HCT253B*	dual 4-input multiplexer; 3-state	16	MSI
HC/HCT257*	quad 2-input multiplexer; 3-state	16	MSI
HC/HCT258	quad 2-input multiplexer; 3-state; inverting	16	MSI
HC/HCT354*	8-input multiplexer/register with transparent latches; 3-state	20	MSI
HC/HCT356*	8-input multiplexer/register; 3-state	20	MSI
Decoders/demultiplexers			
HC/HCT42	BCD to decimal decoder (1-of-10)	16	MSI
HC/HCT137	3-to-8 line decoder/demultiplexer with address latches	16	MSI
HC/HCT138	3-to-8 line decoder/demultiplexer; inverting	16	MSI
HC/HCT139	dual 2-to-4 line decoder/demultiplexer	16	MSI
HC/HCT147	10-to-4 line priority encoder	16	MSI
HC/HCT154	4-to-6 line decoder/demultiplexer	24	MSI
HC/HCT237	3-to-8 line decoder/demultiplexer with address latches	16	MSI
HC/HCT238	3-to-8 line decoder/demultiplexer	16	MSI
HC/HCT4511	BCD to 7-segment latch/decoder/driver	16	MSI
HC/HCT4514	4-to-16 line decoder/demultiplexer with input latches	24	MSI
HC/HCT4515	4-to-16 line decoder/demultiplexer with input latches; inverting	24	MSI
HC/HCT4543	BCD to 7-segment latch/decoder/driver for LCDs	16	MSI
Switches/multiplexers/demultiplexers			
HC/HCT4016	quad bilateral switches (uncompensated switches)	14	SSI
HC/HCT4051	8-channel analog multiplexer/demultiplexer	16	MSI
HC/HCT4052	dual 4-channel analog multiplexer/demultiplexer	16	MSI
HC/HCT4053	triple 2-channel analog multiplexer/demultiplexer	16	MSI
HC/HCT4066	quad bilateral switches	14	SSI
HC/HCT4067	16-channel analog multiplexer/demultiplexer	24	SSI
HC/HCT4316	quad bilateral switches; with separate analog ground	16	MSI
HC/HCT4351	8-channel analog multiplexer/demultiplexer with latch	20	MSI
HC/HCT4352	dual 4-channel analog multiplexer/demultiplexer with latch	20	MSI
HC/HCT4353	triple 2-channel analog multiplexer/demultiplexer with latch	20	MSI
Bus transceivers			
HC/HCT242*	quad bus transceiver; 3-state; inverting	14	MSI
HC/HCT243*	quad bus transceiver; 3-state	14	MSI
HC/HCT245*	octal bus transceiver; 3-state	20	MSI
HC/HCT640*	octal bus transceiver; 3-state; inverting	20	MSI
HC/HCT643*	octal bus transceiver; 3-state; true/inverting	20	MSI
HC/HC/646*	octal bus transceiver/register; 3-state	24	MSI
HC/HCT648*	octal bus transceiver/register; 3-state; inverting	24	MSI

* Types with a bus-driver output stage.

Type numbers have a suffix which signifies the type of package:
P = plastic DIL; T = plastic SO mini-pack

type no.	description	pins	classification
Schmitt triggers			
HC/HCT14	hex inverting Schmitt trigger	14	SSI
HC/HCT132	quad 2-input NAND Schmitt trigger	14	SSI
One-shot multivibrators			
HC/HCT123	dual retriggerable monostable multivibrator with reset	16	MSI
HC/HCT221	dual non-retriggerable monostable multivibrator with reset	16	MSI
HC/HCT423	dual retriggerable monostable multivibrator with reset	16	MSI
HC/HCT4538	dual retriggerable precision monostable multivibrator	14	MSI
Miscellaneous			
HC/HCT297	digital phase-locked-loop filter	16	MSI
HC/HCT4046A	phase-locked-loop with VCO	16	MSI
HC/HCT7046A	phase-locked-loop with lock detector	16	MSI

* Types with a bus-driver output stage.

HCMOS 74HC/HCT/HCU FAMILY

type no.	description
HC/HCT00	quad 2-input NAND gate
HC/HCT02	quad 2-input NOR gate
HC/HCT03	quad 2-input NAND gate (with open drain outputs)
HC/HCT04	hex inverter
HCU04	hex inverter (unbuffered)
HC/HCT08	quad 2-input AND gate
HC/HCT10	triple 3-input NAND gate
HC/HCT11	triple 3-input AND gate
HC/HCT14	hex inverting Schmitt trigger
HC/HCT20	dual 4-input NAND gate
HC/HCT21	dual 4-input AND gate
HC/HCT27	triple 3-input NOR gate
HC/HCT30	8-input NAND gate
HC/HCT32	quad 2-input OR gate
HC/HCT42	BCD to decimal decoder (1-of-10)
HC58	dual AND-OR gate
HC/HCT73	dual JK flip-flop with reset; negative-edge trigger; supply on centre pins
HC/HCT74	dual D-type flip-flop with set and reset; positive-edge trigger
HC/HCT75	quad bistable transparent latch
HC/HCT85	4-bit magnitude comparator
HC/HCT86	quad 2-input EXCLUSIVE-OR gate
HC/HCT93	4-bit binary ripple counter
HC/HCT107	dual JK flip-flop with reset; negative-edge trigger
HC/HCT109	dual J$\overline{K}$ flip-flop with set and reset; positive-edge trigger
HC/HCT112	dual JK flip-flop with set and reset; negative-edge trigger
HC/HCT123	dual retriggerable monostable multivibrator with reset
HC/HCT125*	quad buffer/line driver; 3-state; output enable active LOW
HC/HCT126*	quad buffer/line driver; 3-state; output enable active HIGH
HC/HCT132	quad 2-input NAND Schmitt trigger
HC/HCT137	3-to-8 line decoder/demultiplexer with address latches
HC/HCT138	3-to-8 line decoder/demultiplexer; inverting
HC/HCT139	dual 2-to-4 line decoder/demultiplexer
HC/HCT147	10-to-4 line priority encoder
HC/HCT151	8-input multiplexer
HC/HCT153	dual 4-input multiplexer
HC/HCT154	4-to-16 line decoder/demultiplexer
HC/HCT157	quad 2-input multiplexer
HC/HCT158	quad 2-input multiplexer; inverting
HC/HCT160	presettable synchronous BCD decade counter; asynchronous reset
HC/HCT161	presettable synchronous 4-bit binary counter; asynchronous reset

* Types with a bus driver output stage.

type no.	description
HC/HCT162	presettable synchronous BCD decade counter; synchronous reset
HC/HCT163	presettable synchronous 4-bit binary counter; synchronous reset
HC/HCT164	8-bit serial-in/parallel-out shift register
HC/HCT165	8-bit parallel-in/serial-out shift register
HC/HCT166	8-bit parallel-in/serial-out shift register; with reset
HC/HCT173*	quad D-type flip-flop; positive-edge trigger; 3-state
HC/HCT174	hex D-type flip-flop with reset; positive-edge trigger
HC/HCT175	quad D-type flip-flop with reset; positive-edge trigger
HC/HCT181	4-bit arithmetic logic unit
HC/HCT182	look-ahead carry generator
HC/HCT190	presettable synchronous BCD decade up/down counter
HC/HCT191	presettable synchronous 4-bit binary up/down counter
HC/HCT192	presettable synchronous BCD decade up/down counter
HC/HCT193	presettable synchronous 4-bit binary up/down counter
HC/HCT194	4-bit bidirectional universal shift register
HC/HCT195	4-bit parallel access shift register
HC/HCT221	dual non-retriggerable monostable multivibrator with reset
HC/HCT237	3-to-8 line decoder/demultiplexer with address latches
HC/HCT238	3-to-8 line decoder/demultiplexer
HC/HCT240*	octal buffer/line driver; 3-state; inverting
HC/HCT241*	octal buffer/line driver; 3-state; output enables active LOW or HIGH
HC/HCT242*	quad bus transceiver; 3-state; inverting
HC/HCT243*	quad bus transceiver; 3-state
HC/HCT244*	octal buffer/line driver; 3-state; output enable active LOW
HC/HCT245*	octal bus transceiver; 3-state
HC/HCT251	8-input multiplexer; 3-state
HC/HCT253B*	dual 4-input multiplexer; 3-state
HC/HCT257*	quad 2-input multiplexer; 3-state
HC/HCT258	quad 2-input multiplexer; 3-state; inverting
HC/HCT259	8-bit addressable latch
HC7266	quad 2-input EXCLUSIVE-NOR gate
HC/HCT273	octal D-type flip-flop with reset; positive-edge trigger
HC/HCT280	9-bit odd/even parity generator/checker
HC/HCT283	4-bit binary full adder with fast carry
HC/HCT297	digital phase-locked-loop filter
HC/HCT299*	8-bit universal shift register; 3-state
HC/HCT354*	8-input multiplexer/register with transparent latches; 3-state
HC/HCT356*	8-input multiplexer/register; 3-state
HC/HCT365*	hex buffer/line driver; 3-state
HC/HCT366*	hex buffer/line driver; 3-state; inverting

* Types with a bus driver output stage.

type no.	description
HC/HCT367*	hex buffer/line driver; 3-state
HC/HCT368*	hex buffer/line driver; 3-state; inverting
HC/HCT373*	octal D-type transparent latch; 3-state
HC/HCT374*	octal D-type flip-flop; positive-edge trigger; 3-state
HC/HCT377	octal D-type flip-flop with data enable; positive-edge trigger
HC/HCT390	dual decade ripple counter
HC/HCT393	dual 4-bit binary ripple counter
HC/HCT423	dual retriggerable monostable multivibrator with reset
HC/HCT533*	octal D-type transparent latch; 3-state; inverting
HC/HCT534*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting
HC/HCT540*	octal buffer/line driver; 3-state; inverting
HC/HCT541*	octal buffer/line driver; 3-state
HC/HCT563*	octal D-type transparent latch; 3-state; inverting; bus oriented pin-out
HC/HCT564*	octal D-type flip-flop; positive-edge trigger; 3-state; inverting; bus oriented pin-out
HC/HCT573*	octal D-type transparent latch; 3-state; bus oriented pin-out
HC/HCT574*	octal D-type flip-flop; positive-edge trigger; 3-state; bus oriented pin-out
HC/HCT583	4-bit BCD full adder with fast carry
HC/HCT597	8-bit shift register with input flip-flops
HC/HCT7597	8-bit shift register with input latches
HC/HCT640*	octal bus transceiver; 3-state; inverting
HC/HCT643*	octal bus transceiver; 3-state; true/inverting
HC/HCT646*	octal bus transceiver/register; 3-state
HC/HCT648*	octal bus transceiver/register; 3-state; inverting
HC/HCT670*	4 x 4 register file; 3-state
HC/HCT688	8-bit magnitude comparator
HC/HCT4002	dual 4-input NOR gate
HC/HCT4015	dual 4-bit serial-in/parallel-out shift register
HC/HCT4016	quad bilateral switches (uncompensated switches)
HC/HCT4017	Johnson decade counter with 10 decoded outputs
HC/HCT4020	14-stage binary ripple counter
HC/HCT4024	7-stage binary ripple counter
HC/HCT4040	12-stage binary ripple counter
HC/HCT4046A	phase-locked-loop with VCO
HC4049	hex inverting HIGH-to-LOW level shifter
HC4050	hex HIGH-to-LOW level shifter
HC/HCT4051	8-channel analog multiplexer/demultiplexer
HC/HCT4052	dual 4-channel analog multiplexer/demultiplexer
HC/HCT4053	triple 2-channel analog multiplexer/demultiplexer
HC/HCT4059	programmable divide-by-n counter
HC/HCT4060	14-stage binary ripple counter with oscillator

* Types with a bus driver output stage.

type no.	description
HC/HCT4066	quad bilateral switches
HC/HCT4067	16-channel analog multiplexer/demultiplexer
HC/HCT4075	triple 3-input OR gate
HC/HCT4094	8-stage shift-and-store bus register
HC/HCT4316	quad bilateral switches; with separate analog ground
HC/HCT4351	8-channel analog multiplexer/demultiplexer with latch
HC/HCT4352	dual 4-channel analog multiplexer/demultiplexer with latch
HC/HCT4353	triple 2-channel analog multiplexer/demultiplexer with latch
HC/HCT4510	BCD up/down counter
HC/HCT4511	BCD to 7-segment latch/decoder/driver
HC/HCT4514	4-to-16 line decoder/demultiplexer with input latches
HC/HCT4515	4-to-16 line decoder/demultiplexer with input latches; inverting
HC/HCT4516	binary up/down counter
HC/HCT4518	dual synchronous BCD counter
HC/HCT4520	dual synchronous 4-bit binary counter
HC/HCT4538	dual retriggerable precision monostable multivibrator
HC/HCT4543	BCD to 7-segment latch/decoder/driver for LCDs
HC/HCT7030	9-bit x 64-word FIFO register; 3-state
HC/HCT7046A	phase-locked-loop with lock detector
HC/HCT40102	8-bit synchronous BCD down counter
HC/HCT40103	8-bit synchronous binary down counter
HC/HCT40104*	4-bit bidirectional universal shift register; 3-state
HC/HCT40105	4-bit x 16-word FIFO register

* Types with a bus driver output stage.

CROSS-REFERENCE 54/74 SERIES TTL TO HIGH-SPEED CMOS

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	HC/HCT no.	FC	PC	function
00	00	Y	Y	quad 2-input NAND gate
02	02	Y	Y	quad 2-input NOR gate
03	03	Y	Y	quad 2-input NAND gate
04	04	Y	Y	hex inverter
05	-			hex inverter; open collector
08	08	Y	Y	quad 2-input AND gate
09	-			quad 2-input AND gate; open collector
10	10	Y	Y	triple 3-input NAND gate
11	11	Y	Y	triple 3-input AND gate
12	-			triple 3-input NAND gate; open collector
13	-			dual 4-input Schmitt trigger
14	14	Y	Y	hex inverting Schmitt trigger
15	-			triple 3-input AND gate; open collector
17	-			hex buffer driver; open collector; high voltage
18	-			dual 4-input Schmitt trigger
20	20	Y	Y	dual 4-input NAND gate
21	21	Y	Y	dual 4-input AND gate
22	-			dual 4-input NAND gate; open collector
24	132	Y	Y	quad 2-input NAND Schmitt trigger
26	-			quad 2-input NAND buffer; open collector
27	27	Y	Y	triple 3-input NOR gate
28	-			quad 2-input NOR buffer
30	30	Y	Y	8-input NAND gate
31	-			delay element
32	32	Y	Y	quad 2-input OR gate
33	-			quad 2-input NOR buffer; open collector
37	-			quad 2-input NAND buffer
38	-			quad 2-input NAND buffer; open collector
40	-			dual 4-input NAND buffer
42	42	Y	Y	BCD to decimal decoder (1-of-10)
47	-			BCD to 7-segment decoder/driver
48	4511	N	N	BCD to 7-segment latch/decoder/driver
49	4511	N	N	BCD to 7-segment latch/decoder/driver
51	-			dual 2-wide, 2-input/3-input AND-OR-INVERT gate
54	-			4-wide, 2-input AND-OR-INVERT gate
55	-			2-wide, 4-input AND-OR-INVERT gate
56	-			divider
57	-			divider
58	58	-	-	dual AND-OR gate
73	73	Y	Y	dual JK flip-flop with reset; negative-edge trigger
74	74	Y	Y	dual D-type flip-flop with set and reset; positive-edge trigger
75	75	Y	Y	quad bistable transparent latch
76	112	N	N	dual JK flip-flop with set and reset; negative-edge trigger
77	-			quad D-type latch
78	112	N	N	dual JK flip-flop with set and reset; negative-edge trigger

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	HC/HCT no.	FC	PC	function
83	283	Y	N	4-bit binary full adder; fast carry
85	85	Y	Y	4-bit magnitude comparator
86	86	Y	Y	quad 2-input EXCLUSIVE-OR gate
89	-			64-bit RAM
90	-			decade counter
91	166	N	N	8-bit shift register; serial-in/serial-out
92	-			divide-by-12 counter
93	93	Y	Y	4-bit binary ripple counter
95	195	N	N	4-bit parallel access shift register
96	-			5-bit shift register
104	-			50 MHz counter
105	-			50 MHz counter
107	107	Y	Y	dual JK flip-flop with reset; negative-edge trigger
109	109	Y	Y	dual JK flip-flop with set and reset; positive-edge trigger
112	112	Y	Y	dual JK flip-flop with set and reset; negative-edge trigger
113	107	N	N	dual JK flip-flop with reset; negative-edge trigger
114	-			dual JK flip-flop; negative-edge trigger; common clocks and clear
122	-			retriggerable, resettable monostable multivibrator
123	123	Y	Y	dual retriggerable monostable multivibrator with reset
124	-			dual voltage-controlled oscillator
125	125	Y	Y	quad buffer/line driver; 3-state
126	126	Y	Y	quad buffer/line driver; 3-state
132	132	Y	Y	quad 2-input NAND Schmitt trigger
133	-			13-input NAND gate
136	-			quad 2-input EXCLUSIVE-OR gate; open collector
137	137	Y	Y	1-to-8 line decoder/demultiplexer with address latches
138	138	Y	Y	3-to-8 line decoder/demultiplexer; inverting
139	139	Y	Y	dual 2-to-4 line decoder/demultiplexer
145	-			1-to-10 decoder/driver; open collector
147	147	Y	Y	10-to-4 line priority encoder
148	-			8-to-3 line octal priority encoder
150	-			16-input multiplexer
151	151	Y	Y	8-input multiplexer
152	151	Y	N	8-input multiplexer
153	153	Y	Y	dual 4-input multiplexer
154	154	Y	Y	4-to-16 line decoder/demultiplexer
155	139	N	N	dual 2-to-4 line decoder/demultiplexer
156	-			dual 1-of-4 decoder/demultiplexer; open collector
157	157	Y	Y	quad 2-input multiplexer
158	158	Y	Y	quad 2-input multiplexer; inverting

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	HC/HCT no.	FC	PC	function
160	160	Y	Y	presettable synchronous BCD decade counter; asynchronous reset
161	161	Y	Y	presettable synchronous 4-bit binary counter; asynchronous reset
162	162	Y	Y	presettable synchronous BCD decade counter; synchronous reset
163	163	Y	Y	presettable synchronous 4-bit binary counter; synchronous reset
164	164	Y	Y	8-bit serial-in/parallel-out shift register
165	165	Y	Y	8-bit parallel-in/serial-out shift register
166	166	Y	Y	8-bit parallel-in/serial-out shift register
168	190	N	N	presettable synchronous BCD decade up/down counter
169	191	N	N	presettable synchronous 4-bit binary up/down counter
170	670	N	N	4 x 4 register file; 3-state
171	-			quad D-type flip-flop
173	173	Y	Y	quad D-type flip-flop; positive-edge trigger; 3-state
174	174	Y	Y	hex D-type flip-flop with reset; positive-edge trigger
175	175	Y	Y	quad D-type flip-flop with reset; positive-edge trigger
181	181	Y	Y	4-bit arithmetic logic unit
182	182	Y	Y	look-ahead carry generator
183	-			dual high speed adder
189	-			64-bit RAM
190	190	Y	Y	presettable synchronous BCD decade up/down counter
191	191	Y	Y	presettable synchronous 4-bit binary up/down counter
192	192	Y	Y	presettable synchronous BCD decade up/down counter
193	193	Y	Y	presettable synchronous 4-bit binary up/down counter
194	194	Y	Y	4-bit bidirectional universal shift register
195	195	Y	Y	4-bit parallel access shift register
196	-			presettable decade counter
197	-			presettable binary counter
200	-			256 x 1 RAM
211	-			16 x 9 RAM
212	-			16 x 9 RAM
213	-			16 x 12 RAM
214	-			1024 x 1 RAM
215	-			1024 x 1 RAM
216	-			64 x 4 RAM
217	-			64 x 4 RAM
218	-			32 x 8 RAM

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	HC/HCT no.	FC	PC	function
219	-			16 x 4 RAM
221	221	Y	Y	dual retriggerable monostable multivibrator with reset
222	40105	N	N	4-bit x 16-word FIFO register
224	40105	N	N	4-bit x 16-word FIFO register
227	40105	N	N	4-bit x 16-word FIFO register
228	40105	N	N	4-bit x 16-word FIFO register
237	237	Y	Y	1-to-8 line decoder/demultiplexer with address latches
238	238	Y	Y	3-to-8 line decoder/demultiplexer
239	-			quad 1-of-4 decoder/demultiplexer
240	240	Y	Y	octal buffer/line driver; 3-state; inverting
241	241	Y	Y	octal buffer/line driver; 3-state
242	242	Y	Y	quad bus transceiver; 3-state; inverting
243	243	Y	Y	quad bus transceiver; 3-state
244	244	Y	Y	octal buffer/line driver; 3-state
245	245	Y	Y	octal bus transceiver; 3-state
247	-			BCD to 7-segment decoder/driver; open collector
248	-			BCD to 7-segment decoder (with 2 kΩ pull-up resistors)
249	-			BCD to 7-segment decoder; open collector
251	251	Y	Y	8-input multiplexer; 3-state
253	253	Y	Y	dual 4-input multiplexer; 3-state
256	-			dual 4-bit addressable latch
257	257	Y	Y	quad 2-input multiplexer; 3-state
258	258	Y	Y	quad 2-input multiplexer; 3-state;
259	259	Y	Y	8-bit addressable latch
260	-			dual 5-input NOR gate
261	-			2-bit by 4-bit parallel binary multipliers
266	7266	N	Y	quad 2-input EXCLUSIVE-NOR gate
273	273	Y	Y	octal D-type flip-flop with reset; positive-edge trigger
275	-			7-bit slice Wallace trees
279	-			quad set-reset latch
280	280	Y	Y	9-bit odd/even parity generator/checker
283	283	Y	Y	4-bit binary full adder with fast carry
289	-			64-bit RAM
290	-			BCD decade counter
292	-			programmable frequency divider/digital timer
293	-			4-bit binary counter
294	-			programmable frequency divider/digital timer
295	195	N	N	4-bit parallel access shift register
297	297	Y	Y	digital phase-locked-loop filter
298	-			quad 2-port register
299	299	Y	Y	8-bit universal shift register; 3-state
311	-			16 x 9 RAM
312	-			16 x 9 RAM
314	-			1024 x 1 RAM
315	-			1024 x 1 RAM

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basic no. LS	HC/HCT no.	FC	PC	function
316	-			64 x 4 RAM
317	-			64 x 4 RAM
318	-			32 x 8 RAM
319	-			16 x 4 RAM
320	-			crystal-controlled oscillator
321	-			crystal-controlled oscillator
322	299	N	N	8-bit universal shift register; 3-state
323	-			8-bit universal shift/store register
324	-			voltage-controlled oscillator
325	-			dual voltage-controlled oscillator
326	-			dual voltage-controlled oscillator
327	-			dual voltage-controlled oscillator
328	-			dual voltage-controlled oscillator
333	-			field programmable logic sequencer
334	-			field programmable logic sequencer
335	-			field programmable logic sequencer
336	-			field programmable logic sequencer
340	240	Y	Y	octal buffer/line driver; 3-state; inverting
341	241	Y	Y	octal buffer/line driver; 3-state
344	244	Y	Y	octal buffer/line driver; 3-state
347	-			BCD to 7-segment decoder/ driver
348	-			8-line to 3-line priority encoder
352	153	N	N	dual 4-input multiplexer
353	253	N	N	dual 4-input multiplexer; 3-state
354	354	Y	Y	8-input multiplexer/register with transparent data latch; 3-state
355	354	N	N	8-input multiplexer/register with transparent data latch; 3-state
356	356	Y	Y	8-input multiplexer/register; 3-state
357	356	N	N	8-input multiplexer/register; 3-state
363	373	Y	Y	octal D-type transparent latch; 3-state
364	374	Y	Y	octal D-type flip flop; positive-edge trigger; 3-state
365	365	Y	Y	hex buffer/line driver with common enable; 3-state
366	366	Y	Y	hex buffer/line driver with common enable; 3-state; inverting
367	367	Y	Y	hex buffer/line driver; 3-state
368	368	Y	Y	hex buffer/line driver; 3-state; inverting
373	373	Y	Y	octal D-type transparent latch; 3-state
374	374	Y	Y	octal D-type flip-flop; positive-edge trigger; 3-state
375	75	Y	N	quad bistable transparent latch
377	377	Y	Y	octal D-type flip-flop with data enable; positive-edge trigger
378	174	N	N	hex D-type flip-flop with reset; positive-edge trigger
379	175	N	N	quad D-type flip-flop with reset; positive-edge trigger

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	HC/HCT no.	FC	PC	function
381	-			arithmetic logic unit/function generator
382	-			arithmetic logic unit/function generator
384	-			8-bit serial/parallel two's compliment multiplier
385	-			quad serial adder/subtractor
386	86	Y	N	quad 2-input EXCLUSIVE-OR gate
388	-			quad D-type flip-flop
390	390	Y	Y	dual decade ripple counter
393	393	Y	Y	dual 4-bit binary ripple counter
395	195	N	N	4-bit parallel access shift register
396	-			octal storage register
398	-			quad 2-input multiplexer
399	157	N	N	quad 2-input multiplexer
422	-			retriggerable monostable multivibrator
423	423	Y	Y	dual retriggerable monostable multivibrator with reset
424	-			clock generator and driver
440	-			quad tridirectional bus transceiver; open collector
441	-			quad tridirectional bus transceiver; inverting; open collector
442	-			quad tridirectional bus transceiver; 3-state
443	-			quad tridirectional bus transceiver; inverting; 3-state
444	-			quad tridirectional bus transceiver; true/inverting; 3-state
445	-			BCD to decimal decoder/driver
446	-			quad bus transceiver
447	-			BCD to 7-segment decoder/driver
448	-			quad tridirectional bus transceiver; true/inverting; open collector
449	-			quad bus transceiver
462	-			fibre optic transmitter
463	-			fibre optic transmitter
465	541	N	N	octal buffer/line driver; 3-state
466	540	N	N	octal buffer/line driver; 3-state; inverting
467	241	Y	N	octal buffer/line driver; 3-state
468	240	Y	N	octal buffer/line driver; 3-state; inverting
481	-			4-bit slice processor element
490	390	N	N	dual decade ripple counter
502	-			8-bit successive approximation register
503	-			8-bit successive approximation register
504	-			12-bit successive approximation register
533	533	Y	Y	octal D-type transparent latch; 3-state; inverting
534	534	Y	Y	octal D-type flip-flop; positive-edge trigger; 3-state; inverting
540	540	Y	Y	octal buffer/line driver; 3-state; inverting
541	541	Y	Y	octal buffer/line driver; 3-state

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic no. LS	HC/HCT no.	FC	PC	function
544	240	N	N	octal buffer/line driver; 3-state; inverting
563	563	Y	Y	octal D-type transparent latch; 3-state; inverting
564	564	Y	Y	octal D-type flip-flop; positive-edge trigger; 3-state; inverting
568	190	N	N	presettable synchronous BCD decade up/down counter
569	191	N	N	presettable synchronous 4-bit binary up/down counter
573	573	Y	Y	octal D-type transparent latch; 3-state
574	574	Y	Y	octal D-type flip-flop; positive-edge trigger; 3-state
590	-			8-bit counter with output register
591	-			8-bit counter with output register
592	-			8-bit counter with input register
593	-			8-bit counter with input register
595	4094	N	N	8-stage shift-and-store bus register
596	4094	N	N	8-stage shift-and-store bus register
597	597	Y	Y	8-bit shift register with input latches
598	-			8-bit shift register with input latches
600	-			memory refresh controller
601	-			memory refresh controller
602	-			memory refresh controller
603	-			memory refresh controller
605	-			octal 2-input multiplexed latches
606	-			octal 2-input multiplexed latches
607	-			octal 2-input multiplexed latches
608	-			memory cycle controller
610	-			memory mapper
612	-			memory mapper
613	-			memory mapper
620	640	N	N	octal bus transceiver; 3-state; inverting
621	-			octal bus transceiver; open collector
622	-			octal bus transceiver; inverting; open collector
623	245	N	N	octal bus transceiver; 3-state
624	-			voltage-controlled oscillator
625	-			voltage-controlled oscillator
626	-			voltage-controlled oscillator
627	-			voltage-controlled oscillator
628	-			voltage-controlled oscillator
629	-			voltage-controlled oscillator
630	-			16-bit error detection and correction circuit
631	-			16-bit error detection and correction circuit
638	-			octal bus transceiver
639	-			octal bus transceiver

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basic no. LS	HC/HCT no.	FC	PC	function
640	640	Y	Y	octal bus transceiver; 3-state; inverting
641	-			octal transceiver; open collector
642	-			octal inverting transceiver; open collector
643	643	Y	Y	octal bus transceiver; 3-state; true/inverting
644	-			octal true/inverting transceiver; open collector
645	245	Y	Y	octal bus transceiver; 3-state
646	646	Y	Y	octal bus transceiver/register; 3-state
647	-			octal transceiver/register; open collector
648	648	Y	Y	octal bus transceiver/register; 3-state; inverting
649	-			octal inverting transceiver/register; open collector
651	-			octal transceiver
652	-			octal transceiver
668	190	N	N	presettable synchronous BCD decade up/down counter
669	191	N	N	presettable synchronous 4-bit binary up/down counter
670	670	Y	Y	4 x 4 register file; 3-state
671	-			4-bit universal shift register/latch; 3-state
672	-			4-bit universal shift register/latch; 3-state
673	-			16-bit serial-in/serial-out shift register; 16-bit parallel storage out
674	-			16-bit parallel-in serial-out shift register
681	-			4-bit parallel binary accumulator
682	688	N	N	8-bit magnitude comparator
683	688	N	N	8-bit magnitude comparator
684	688	N	N	8-bit magnitude comparator
685	688	N	N	8-bit magnitude comparator
686	688	N	N	8-bit magnitude comparator
687	688	N	N	8-bit magnitude comparator
688	688	Y	Y	8-bit magnitude comparator
689	688	N	N	8-bit magnitude comparator
690	-			synchronous decade counter; asynchronous clear
691	-			synchronous 4-bit binary counter; asynchronous clear
692	-			synchronous decade counter; synchronous clear
693	-			synchronous 4-bit binary counter; synchronous clear
696	-			synchronous up/down counter with output register and multiplexed outputs; 3-state
698	-			synchronous up/down counter with output register and multiplexed outputs; 3-state
699	-			synchronous up/down counter with output register and multiplexed outputs; 3-state

CROSS-REFERENCE 4000 SERIES CMOS TO HIGH-SPEED CMOS

FC = function compatible; PC = pin compatible; Y = yes; N = no

basic 4000 no.	HC no.	FC	PC	function
4000	-	-	-	dual 3-input NOR gate and inverter
4001	02	Y	N	quad 2-input NOR gate
4002	4002	Y	Y	dual 4-input NOR gate
4006	-			18-stage static shift register
4007	-			dual complementary pair and inverter
4008	283	Y	N	4-bit binary full adder
4009	-			hex buffer/converter; inverting
4010	-			hex buffer/converter
4011	00	Y	N	quad 2-input NAND gate
4012	20	Y	N	dual 4-input NAND gate
4013	74	N	N	dual D-type flip-flop with set and reset; positive-edge trigger
4014	-			8-bit static shift register
4015	4015	Y	Y	dual 4-bit serial-in/parallel-out shift register
4016	4016/4316	Y	Y	quad bilateral switches
4017	4017	Y	Y	Johnson decade counter with 10 decoded outputs
4018	-			presettable divide-by-n counter
4019	157	N	N	quad 2-input multiplexer
4020	4020	Y	Y	14-stage binary ripple counter
4021	166	N	N	8-bit parallel-in/serial-out shift register
4022	-			4-stage divide-by-8 Johnson counter
4023	10	Y	N	triple 3-input NAND gate
4024	4024	Y	Y	7-stage binary ripple counter
4025	27	Y	N	triple 3-input NOR gate
4026	-			decoded counter/divider with 7-segment outputs
4027	109	Y	N	dual JK- flip-flop with set and reset; positive-edge trigger
4028	42	Y	N	BCD to decimal decoder (1-of-10)
4029	-			synchronous up/down - binary/decade counter
4030	86	Y	N	quad 2-input EXCLUSIVE-OR gate
4031	-			64-stage static shift register
4032	-			triple serial adder, positive logic
4033	-			decoder counter/divider with 7-segment outputs; ripple blanking
4034	-			8 stage static bidirectional parallel/serial input/output bus register
4035	-			4-bit universal shift register
4037	-			triple AND/OR bi-phase pair
4038	-			triple serial adder; negative logic
4040	4040	Y	Y	12-stage binary ripple counter
4041	-			quad true/complement buffer
4042	-			quad D-latch
4043	-			quad R/S latch; 3-state
4044	-			quad R/S latch; 3-state
4045	-			21-stage counter
4046A	4046	Y	Y	phase-locked-loop with VCO
4047	-			monostable/astable multivibrator
4048	-			multi-function expandable 8-input
4049	4049	Y	Y	hex inverting HIGH-to-LOW level shifter

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basic 4000 no.	HC no.	FC	PC	function
4050	4050	Y	Y	hex HIGH-to-LOW level shifter
4051	4051/4351	Y	Y	8-channel analog multiplexer/demultiplexer
4052	4052/4352	Y	Y	dual 4-channel analog multiplexer/ demultiplexer
4053	4053/4353	Y	Y	triple 2-channel analog multiplexer/ demultiplexer
4054	-			4-segment LCD driver
4055	4543	N	N	BCD to 7-segment latch/decoder/driver for LCDs
4056	-			BCD to 7-segment decoder/driver with strobed latch function; LCD driver
4057	-			4-bit arithmetic logic unit
4059	4059	Y	Y	programmable divide-by-n counter
4060	4060	Y	Y	14-stage binary ripple counter with oscillator
4062	-			200-stage dynamic shift register
4063	85	N	N	4-bit magnitude comparator
4066	4066	Y	Y	quad bilateral switches
4067	4067	Y	Y	16-channel analog multiplexer/demultiplexer
4068	30	Y	N	8-input NAND gate
4069	04	Y	Y	hex inverter
4070	86	Y	N	quad 2-input EXCLUSIVE-OR gate
4071	32	Y	N	quad 2-input OR gate
4072	-			dual 4-input OR gate
4073	11	Y	N	triple 3-input AND gate
4075	4075	Y	Y	triple 3-input OR gate
4076	173	Y	Y	quad D-type flip-flop; positive-edge trigger; 3-state
4077	7266	Y	Y	quad EXCLUSIVE-NOR gate
4078	-			8-input NOR gate
4081	08	Y	N	quad 2-input AND gate
4082	21	Y	N	dual 4-input AND gate
4085	-			dual 2-wide 2-input AND-OR-INVERT gate
4086	-			4-wide 2-input AND-OR-INVERT gate
4089	-			binary rate multiplier
4093	132	Y	N	quad 2-input NAND Schmitt trigger
4094	4094	Y	Y	8-stage shift-and-store bus register
4095	-			gated JK master slave flip-flop
4096	-			gated JK master slave flip-flop; inverting and non-inverting inputs
4097	-			differential 8-channel multiplexer/ demultiplexer
4098	423	Y	N	dual retriggerable monostable multivibrator with reset
4099	259	N	N	8-bit addressable latch
4104	-	-	-	quad low-to-high voltage translator; 3-state
4500	-			industrial control unit
4501	-			triple gate
4502	368	N	N	hex buffer/line driver; 3-state; inverting
4503	367	Y	Y	hex buffer/line driver; 3-state
4504	-			hex LOW-to-HIGH level shifter
4505	-			64-bit static read/write RAM
4506	-			dual expandable AND-OR-INVERT gate
4507	86	Y	N	quad 2-input EXCLUSIVE-OR gate
4508	-			dual 4-bit latch

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basic 4000 no.	HC no.	FC	PC	function
4510	4510	Y	Y	BCD up/down counter
4511	4511	Y	Y	BCD to 7-segment latch/decoder/driver
4512	251	N	N	8-input multiplexer; 3-state
4513	-			BCD to 7-segment latch/decoder/driver; ripple blanking
4514	4514	Y	Y	4-to-16 line decoder/demultiplexer with input latches
4515	4515	Y	Y	4-to-16 decoder/demultiplexer with input latches
4516	4516	Y	Y	binary up/down counter
4517	-			dual 64-bit static shift register
4518	4518	Y	Y	dual synchronous BCD counter
4519	157	N	N	quad 2-input multiplexer
4520	4520	Y	Y	dual 4-bit synchronous binary counter
4521	-			24-stage frequency divider
4522	-			programmable 4-bit BCD down counter
4524	-			256 x 4 ROM
4526	-			programmable 4-bit binary down counter
4527	-			BCD rate multiplier
4528	423	N	N	dual retriggerable monostable multivibrator with reset
4529	4052	N	N	dual 4-channel analog multiplexer/ demultiplexer
4530	-			dual 5-input majority logic gate
4531	-			13-input parity checker/generator
4532	-			8-input priority encoder
4534	-			real time 5-decade counter
4536	-			programmable timer
4537	-			256 x 1 static RAM
4538	4538	Y	Y	dual retriggerable precision monostable multivibrator
4539	153	Y	Y	dual 4-channel multiplexer/demultiplexer
4541	-			programmable timer
4543	4543	Y	Y	BCD to 7-segment latch/decoder/driver for LCDs
4544	-			BCD to 7-segment decoder/driver/latch; ripple blanking
4547	-			BCD to 7-segment decoder/driver/latch; high current
4549	-			successive approximation register
4551	-			quad 2-channel analog multiplexer
4552	-			64 x 4 static RAM
4553	-			3-digit BCD counter
4554	-			2 x 2-bit binary multiplier
4555	139	Y	Y	dual 2-to-4 line decoder/demultiplexer
4556	-			dual 1-of-4 decoder/demultiplexer; inverting
4557	-			1-to-64 bit variable length shift register
4558	-			BCD to 7-segment decoder
4559	-			successive approximation register
4560	-			NBCD adder
4561	-			9's complementer
4562	-			128-bit static shift register
4566	-			time base generator
4568	-			phase comparator, programmable counter

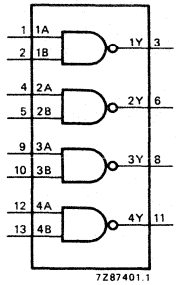
FC = function compatible; PC = pin compatible; Y = yes; N = no

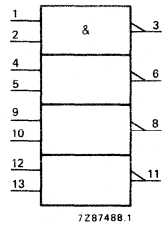
basic 4000 no.	HC no.	FC	PC	function
4569	-			dual programmable BCD/binary counter
4572	-			hex gate
4580	-			4 x 4 multiport register
4581	181	Y	Y	4-bit arithmetic logic unit
4582	182	Y	Y	look-ahead carry generator
4583	-			dual Schmitt trigger
4584	14	Y	Y	hex inverting Schmitt trigger
4585	85	Y	Y	4-bit magnitude comparator
4597	-			8-bit bus-compatible counter/latch
4598	-			8-bit bus-compatible addressable latch
4599	249	N	Y	8-bit addressable latch
40097	367	Y	Y	hex buffer/line driver; 3-state
40098	368	Y	Y	hex buffer/line driver; 3-state; inverting
40100	-			32-stage left/right shift register
40101	280	N	N	9-bit odd/even parity generator/checker
40102	40102	Y	Y	8-bit synchronous BCD down counter
40103	40103	Y	Y	8-bit binary down counter
40104	40104	Y	Y	4-bit bidirectional universal shift register; 3-state
40105	40105	Y	Y	4-bit x 16-word FIFO register
40106	14	Y	Y	hex inverting Schmitt trigger
40107	-			dual 2-input NAND buffer/driver
40108	-			4 x 4 multiport register
40109	-			quad LOW-to-HIGH level shifter
40110	-			decade up/down counter/decoder/latch/driver
40115	-			8-bit universal bidirectional CMOS/TTL level converter
40116	-			8-bit universal bidirectional CMOS/TTL level converter
40147	174	Y	Y	hex D-type flip-flop with reset; positive-edge trigger
40160	160	Y	Y	presettable synchronous BCD decade counter; asynchronous reset
40161	161	Y	Y	presettable synchronous 4-bit binary counter; asynchronous reset
40162	162	Y	Y	presettable synchronous BCD decade counter; synchronous reset
40163	163	Y	Y	presettable synchronous 4-bit binary counter; synchronous reset
40174	174	Y	Y	hex D-type flip-flop with reset; positive-edge trigger
40175	175	Y	Y	quad D-type flip-flop with reset; positive-edge trigger
40181	181	Y	Y	4-bit arithmetic logic unit
40182	182	Y	Y	look-ahead carry generator
40192	192	Y	Y	presettable synchronous BCD decade up/down counter
40193	193	Y	Y	presettable synchronous 4-bit binary up/down counter
40194	194	Y	Y	4-bit bidirectional universal shift register
40208	-			4 x 4 multiport register
40240	240	Y	Y	octal buffer/line driver; 3-state; inverting
40244	244	Y	Y	octal buffer/line driver; 3-state
40245	245	Y	Y	octal bus transceiver; 3-state
40373	373	Y	Y	octal D-type transparent latch; 3-state
40374	374	Y	Y	octal D-type flip-flop; positive-edge trigger; 3-state

FUNCTIONAL DIAGRAMS

IEC LOGIC DIAGRAMS

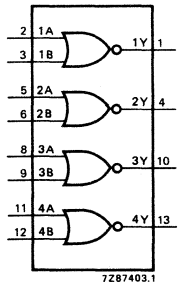
HC/HCT00

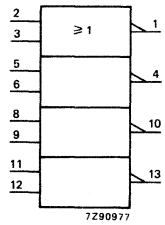




Quad 2-input NAND gate

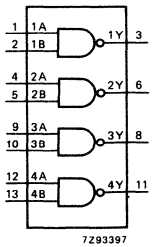
HC/HCT02

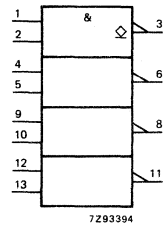




Quad 2-input NOR gate

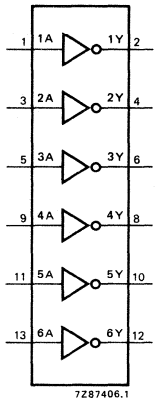
HC/HCT03

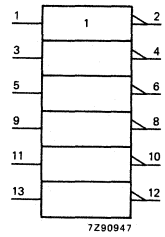




Quad 2-input NAND gate

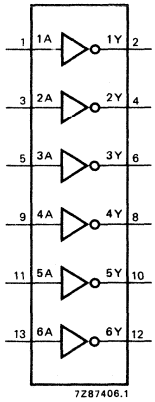
HC/HCT04

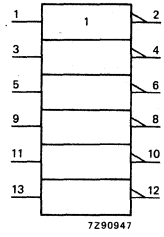




Hex inverter

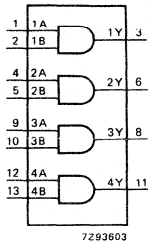
HCU04

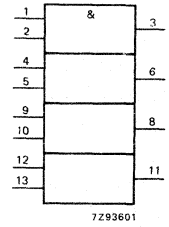




Hex inverter (unbuffered)

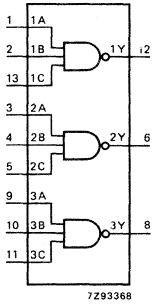
HC/HCT08

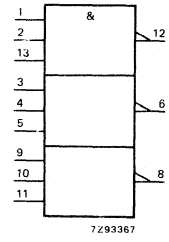




Quad 2-input AND gate

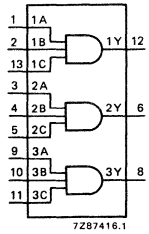
HC/HCT10

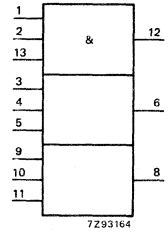




Triple 3-input NAND gate

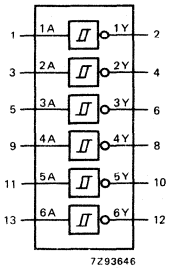
HC/HCT11

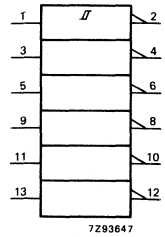




Triple 3-input AND gate

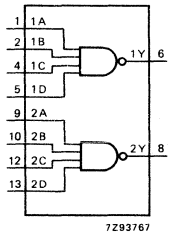
HC/HCT14

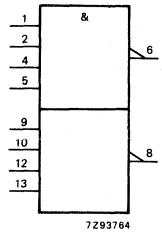




Hex inverting Schmit trigger

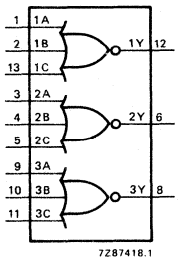
HC/HCT20

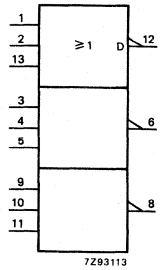




Dual 4-bit NAND gate

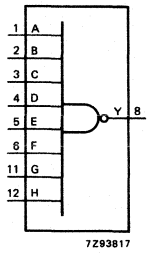
HC/HCT27

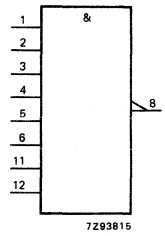




Triple 3-input NOR gate

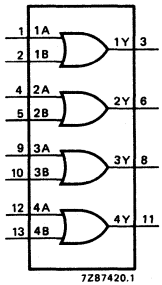
HC/HCT30

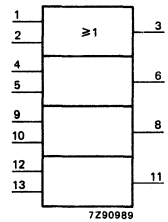




8-input NAND gate

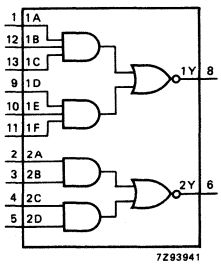
HC/HCT32





Quad 2-input OR gate

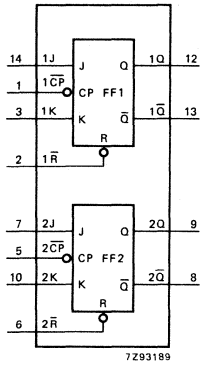
HC58

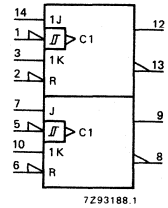


IEC SYMBOL
IN
PROGRESS

Dual AND-OR gate

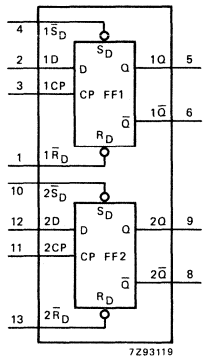
HC/HCT73

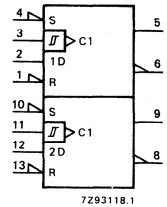




Dual JK flip-flop with reset; negative-edge trigger

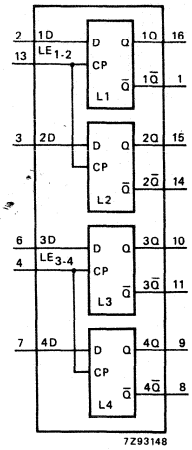
HC/HCT74

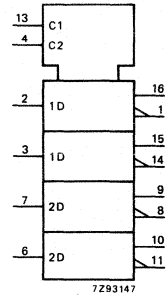




Dual D-type flip-flop with set and reset; positive-edge trigger

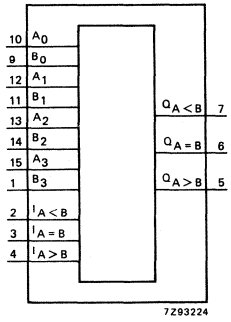
HC/HCT75

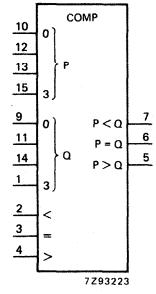




Quad bistable transparent latch

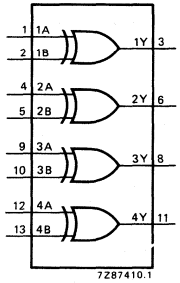
HC/HCT85

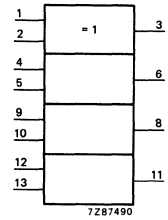




4-bit magnitude comparator

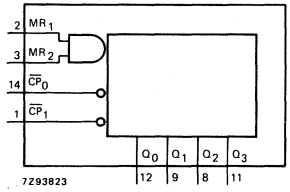
HC/HCT86

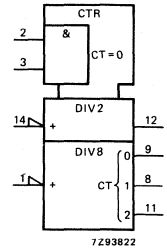




Quad 2-input EXCLUSIVE–OR gate

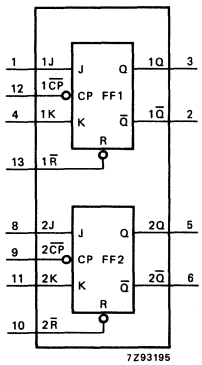
HC/HCT93

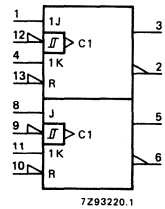




4-bit binary ripple counter

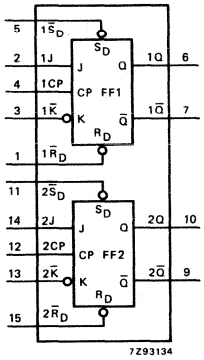
HC/HCT107

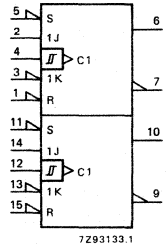




Dual JK flip-flop with reset; negative-edge trigger

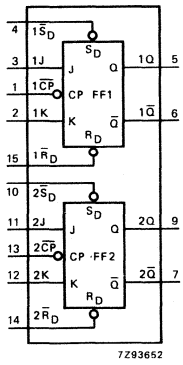
HC/HCT109

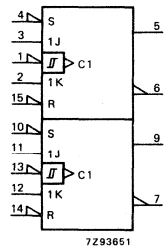




Dual J$\overline{K}$ flip-flop with set and reset; positive-edge trigger

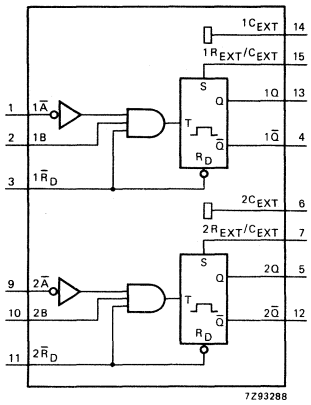
HC/HCT112

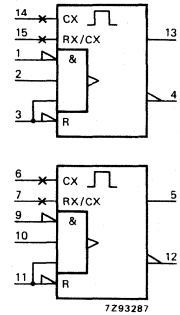




Dual JK flip-flop with set and reset; negative-edge trigger

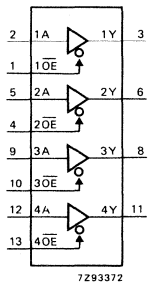
HC/HCT123

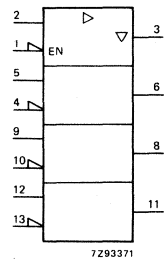




Dual retriggerable monostable multivibrator with reset

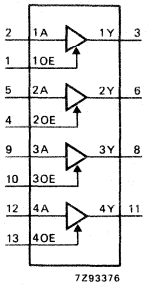
HC/HCT125

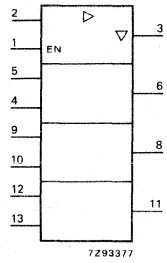




Quad buffer/line driver; 3-state

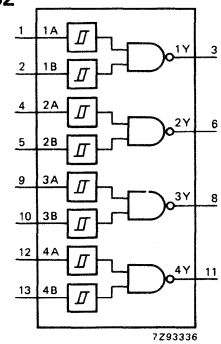
HC/HCT126

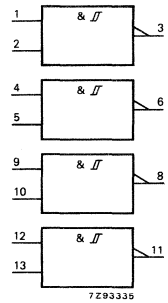




Quad buffer/line driver; 3-state

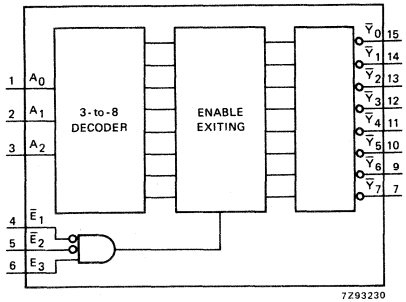
HC/HCT132

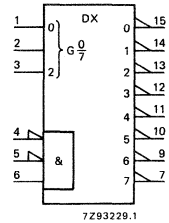




Quad 2-input NAND Schmitt trigger

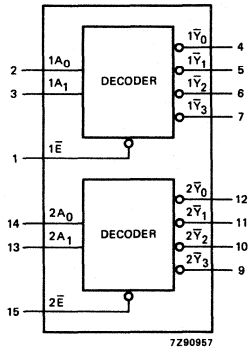
HC/HCT138

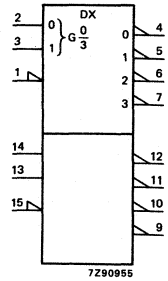




3-to-8 line decoder/demultiplexer; inverting

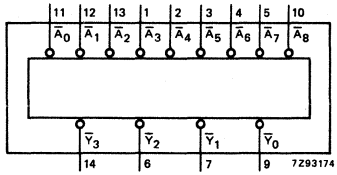
HC/HCT139

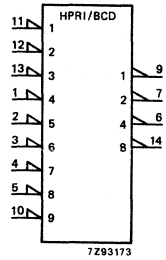




Dual 2-to-4 line decoder/demultiplexer

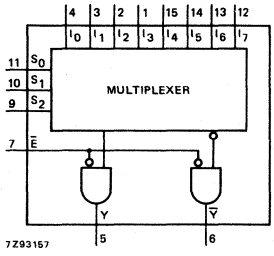
HC/HCT147

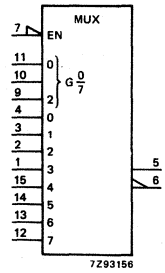




10-to-4 line priority encoder

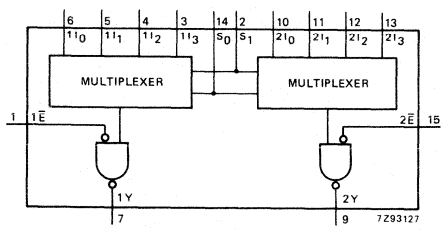
HC/HCT151

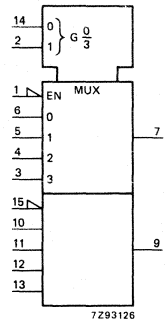




8-input multiplexer

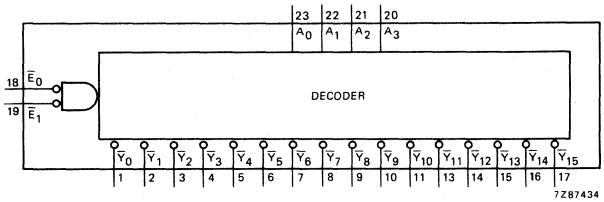
HC/HCT153

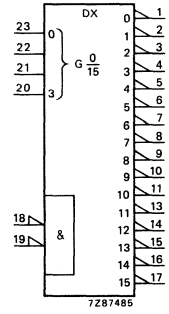




Dual 4-input multiplexer

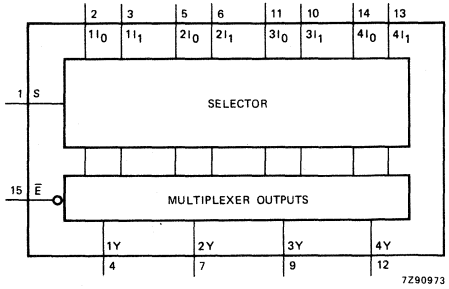
HC/HCT154

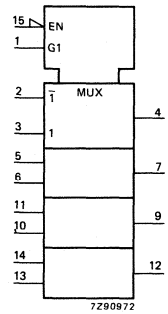




4-to-16 line decoder/demultiplexer

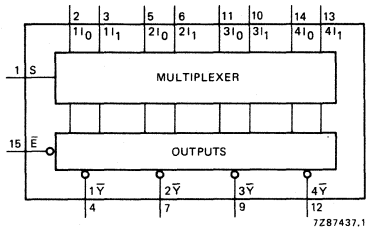
HC/HCT157

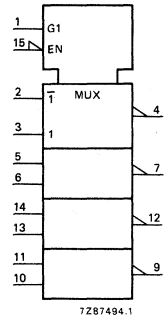




Quad 2-input multiplexer

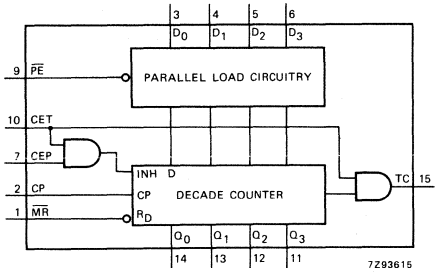
HC/HCT158

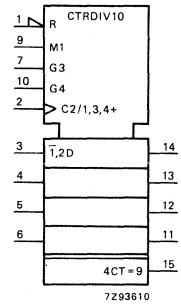




Quad 2-input multiplexer; inverting

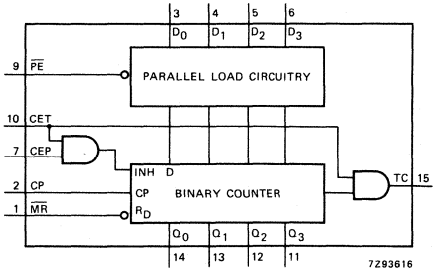
HC/HCT160

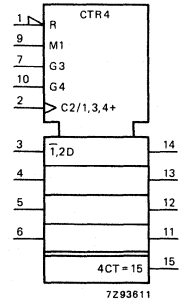




Presettable synchronous BCD decade counter; asynchronous reset

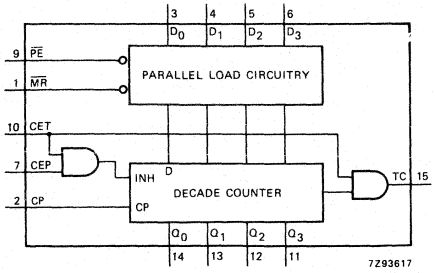
HC/HCT161

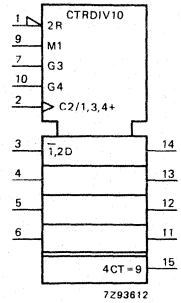




Presettable synchronous 4-bit binary counter; asynchronous reset

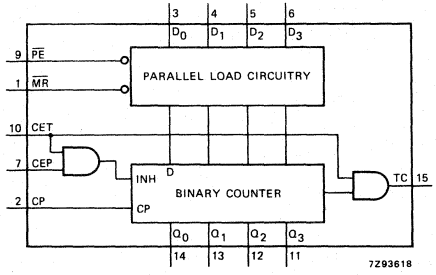
HC/HCT162

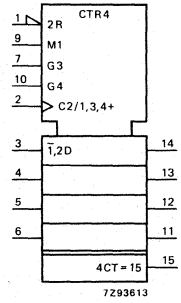




Presettable synchronous BCD decade counter; synchronous reset

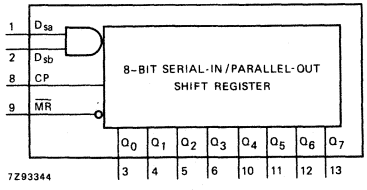
HC/HCT163

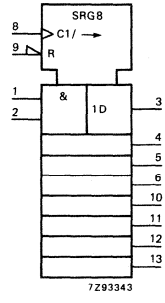




Presettable synchronous 4-bit binary counter; synchronous reset

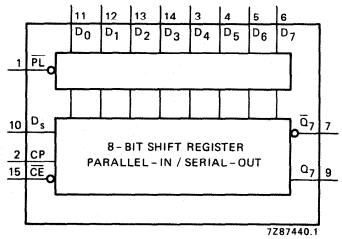
HC/HCT164

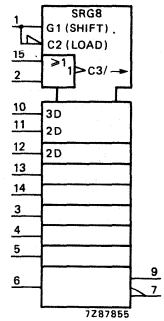




8-bit serial-in/parallel-out shift register

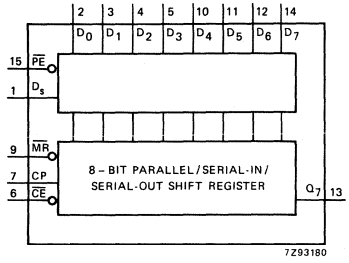
HC/HCT165

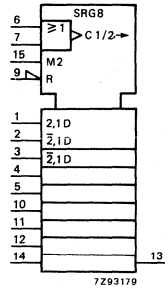




8-bit parallel-in/serial-out shift register

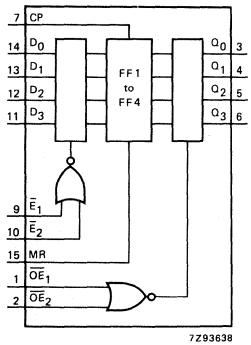
HC/HCT166

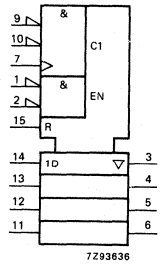




8-bit parallel-in/serial-out shift register

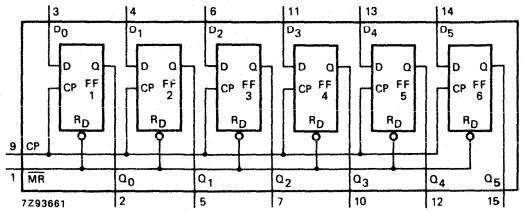
HC/HCT173

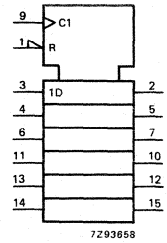




Quad D-type flip-flop; positive-edge trigger; 3-state

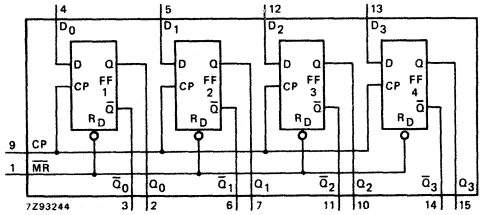
HC/HCT174

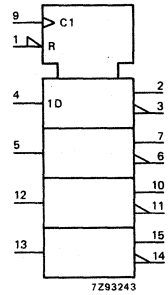




Hex D-type flip-flop with reset; positive-edge trigger

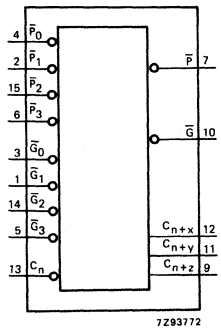
HC/HCT175

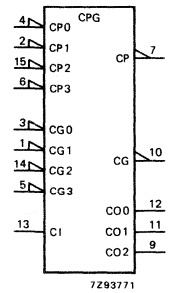




Quad D-type flip-flop with reset; positive-edge trigger

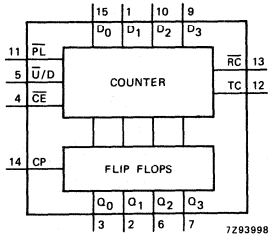
HC/HCT182

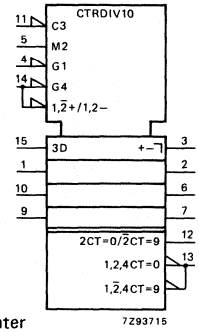




Look-ahead carry generator

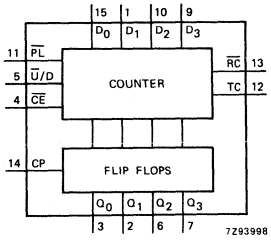
HC/HCT190

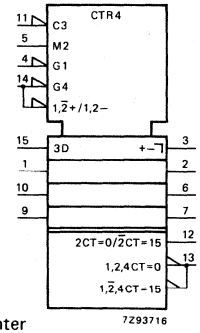




Presettable synchronous BCD decade up/down counter

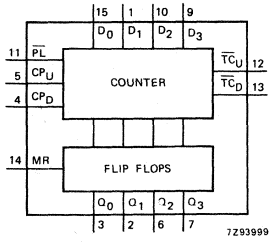
HC/HCT191

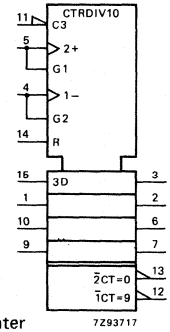




Presettable synchronous 4-bit binary up/down counter

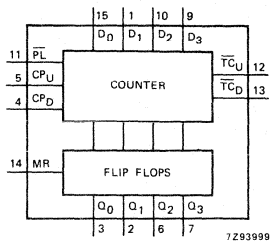
HC/HCT192

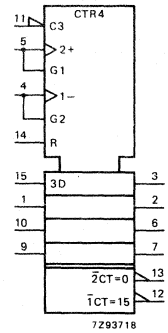




Presettable synchronous BCD decade up/down counter

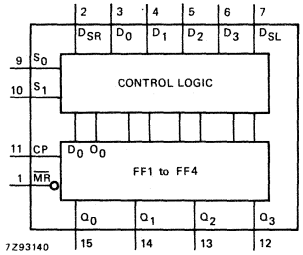
HC/HCT193

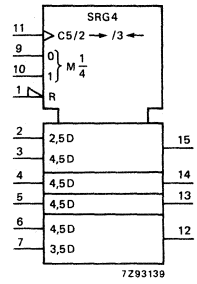




Presettable synchronous 4-bit binary up/down counter

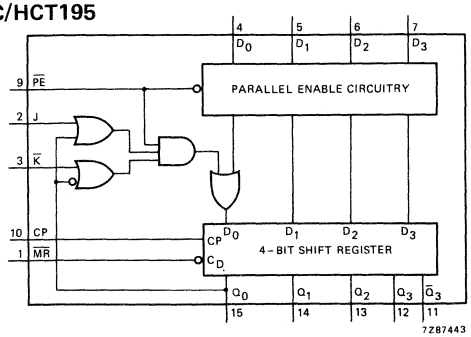
HC/HCT194

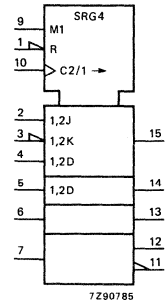




4-bit bidirectional universal shift register

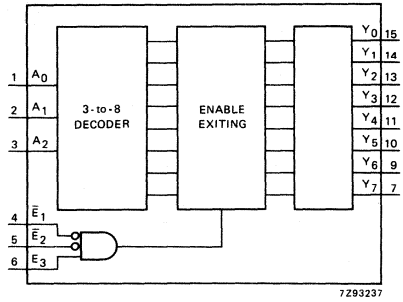
HC/HCT195

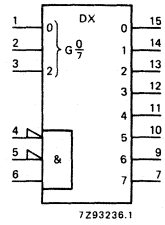




4-bit parallel access shift register

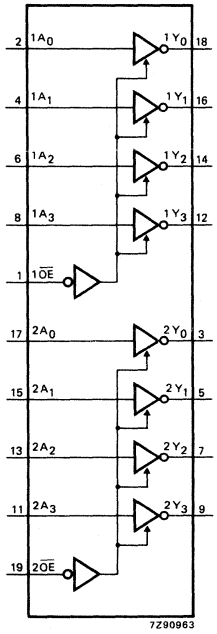
HC/HCT238

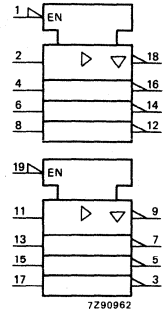




3-to-8 line decoder/demultiplexer

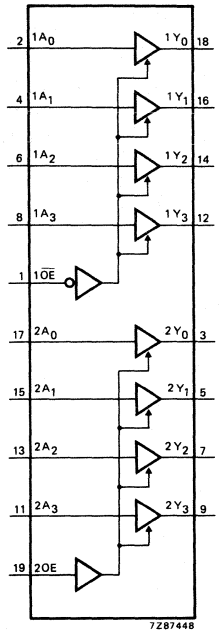
HC/HCT240

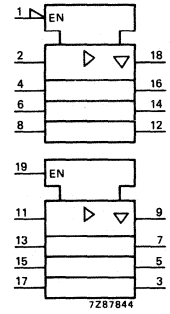




Octal buffer/line driver; 3-state; inverting

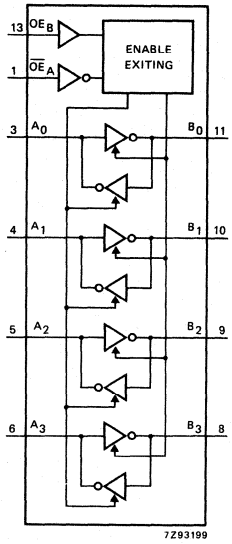
HC/HCT241

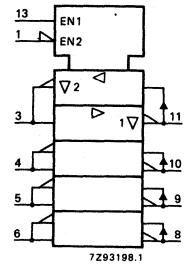




Octal buffer/line driver; 3-state

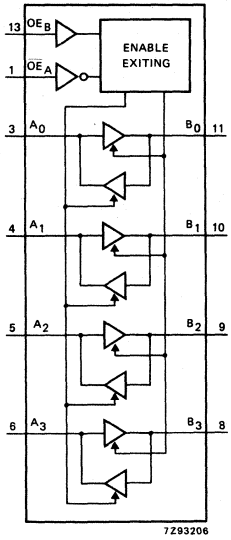
HC/HCT242

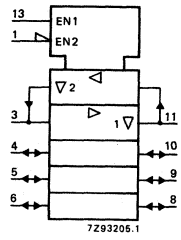




Quad bus transceiver; 3-state; inverting

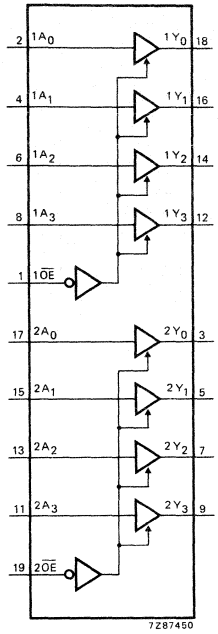
HC/HCT243

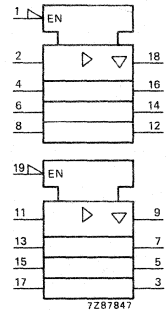




Quad bus transceiver; 3-state

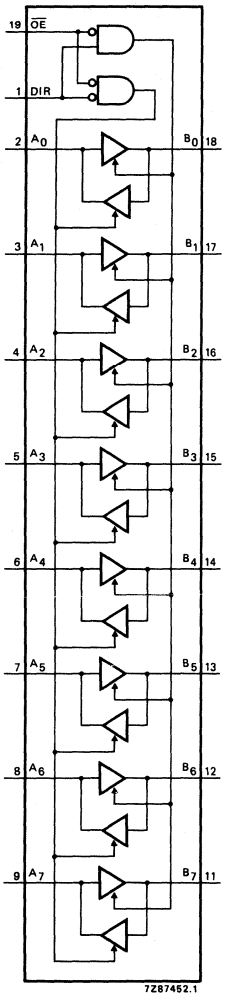
HC/HCT244

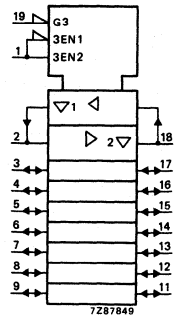




Octal buffer/line driver; 3-state

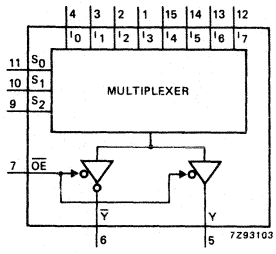
HC/HCT245

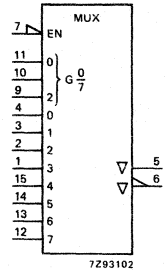




Octal bus transceiver; 3-state

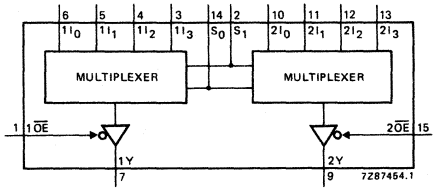
HC/HCT251

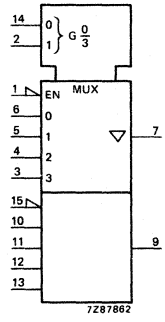




8-input multiplexer; 3-state

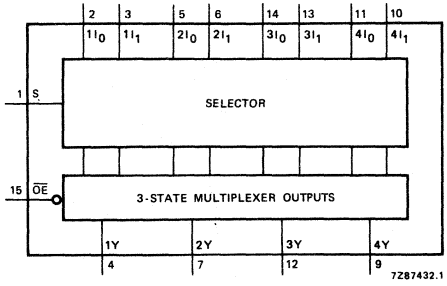
HC/HCT253B

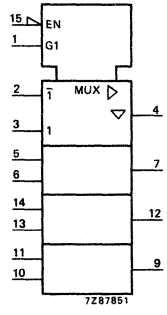




Dual 4-input multiplexer; 3-state

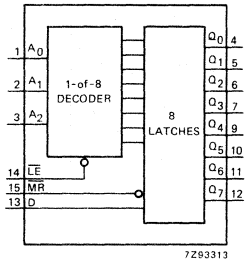
HC/HCT257

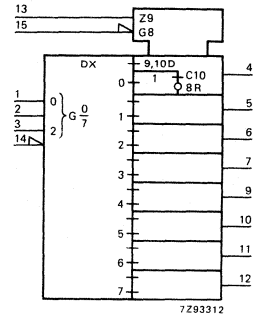




Quad 2-input multiplexer; 3-state

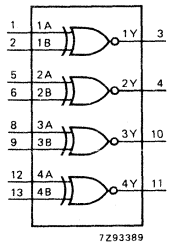
HC/HCT259

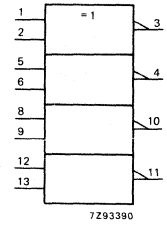




8-bit addressable latch

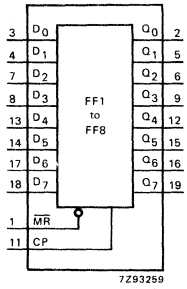
HC7266

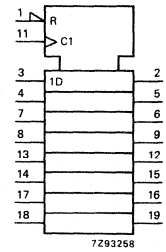




Quad 2-input EXCLUSIVE-NOR gate

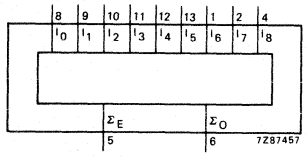
HC/HCT273

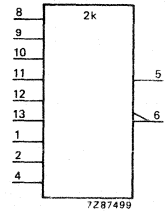




Octal D-type flip-flop with reset; positive-edge trigger

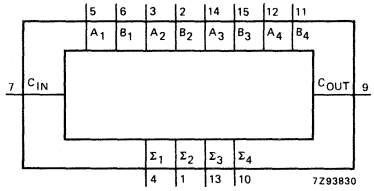
HC/HCT280

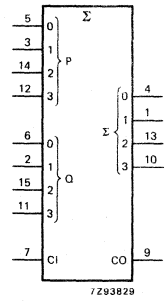




9-bit odd/even parity generator/checker

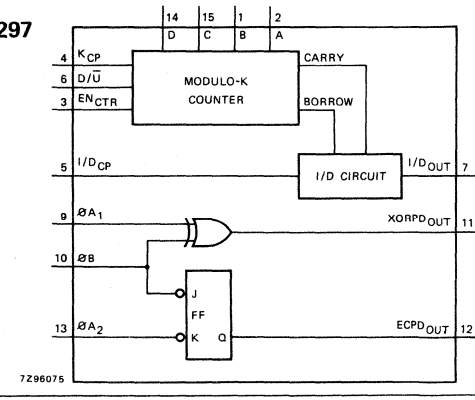
HC/HCT283





4-bit binary full adder with fast carry

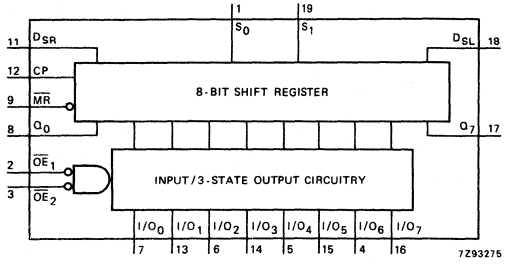
HC/HCT297

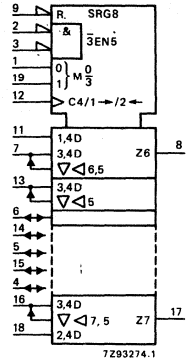


IEC SYMBOL
IN
PROGRESS

Digital phase-locked-loop filter

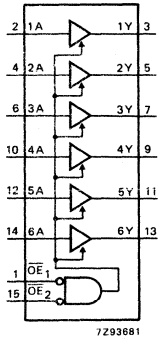
HC/HCT299

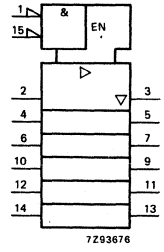




8-bit universal shift register; 3-state

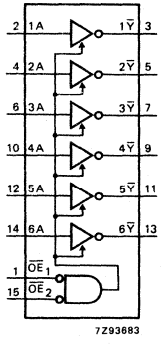
HC/HCT365

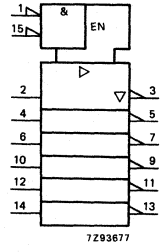




Hex buffer/line driver; 3-state

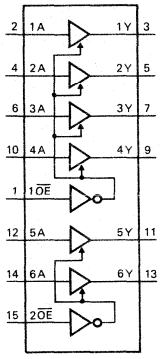
HC/HCT366

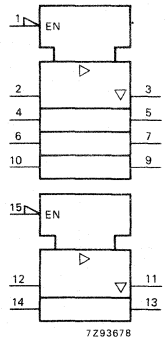




Hex buffer/line driver; 3-state; inverting

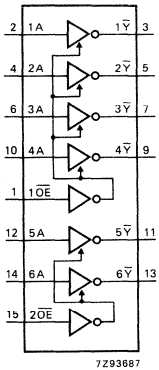
HC/HCT367

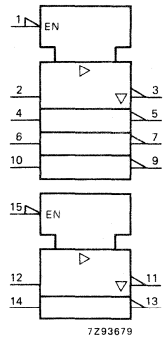




Hex buffer/line driver; 3-state

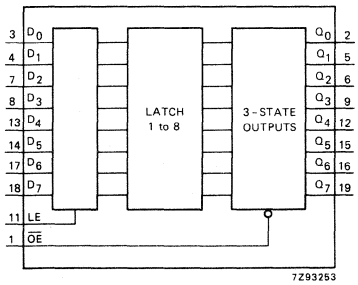
HC/HCT368

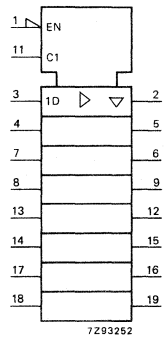




Hex buffer/line driver; 3-state; inverting

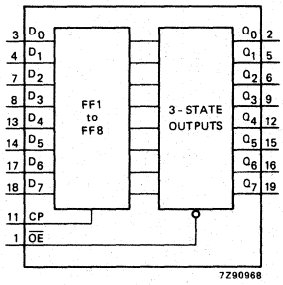
HC/HCT373

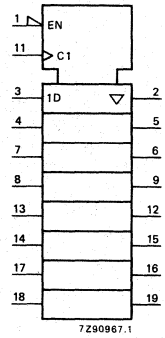




Octal D-type transparent latch; 3-state

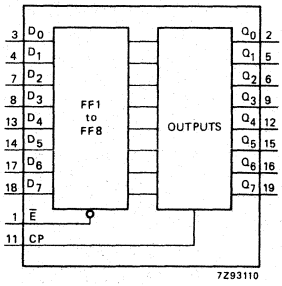
HC/HCT374

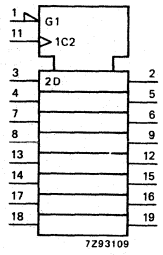




Octal D-type flip-flop; positive-edge trigger; 3-state

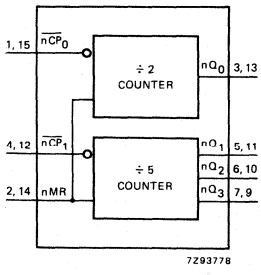
HC/HCT377

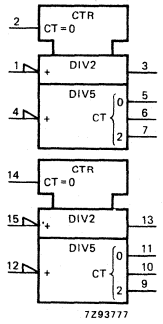




Octal D-type flip-flop with data enable; positive-edge trigger

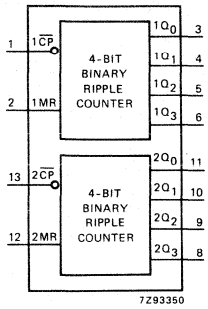
HC/HCT390

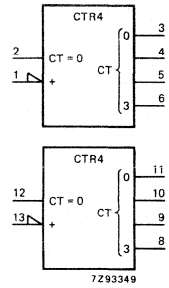




Dual decade ripple counter

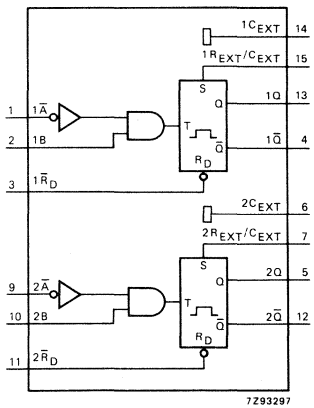
HC/HCT393

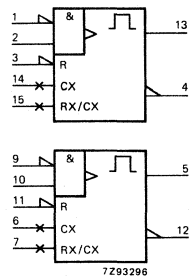




Dual 4-bit binary ripple counter

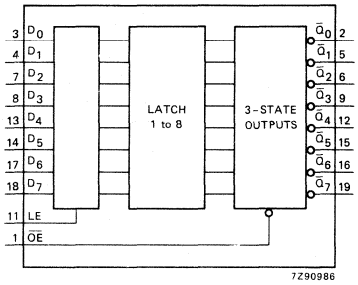
HC/HCT423

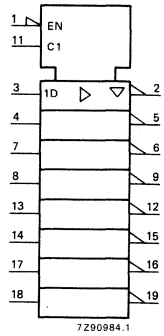




Dual retriggerable monostable multivibrator with reset

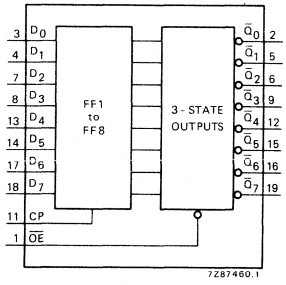
HC/HCT533

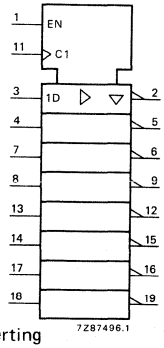




Octal D-type transparent latch; 3-state; inverting

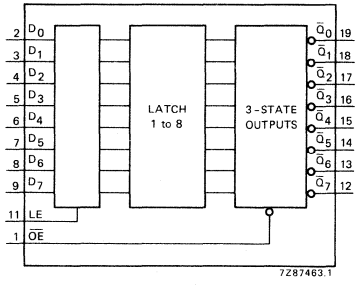
HC/HCT534

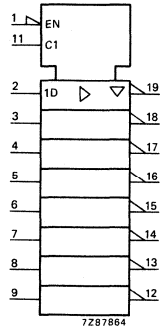




Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

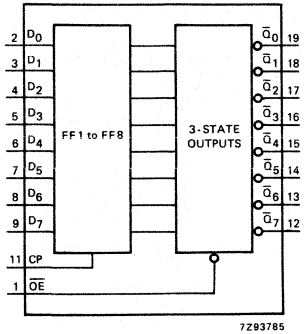
HC/HCT563

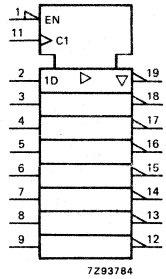




Octal D-type transparent latch; 3-state; inverting

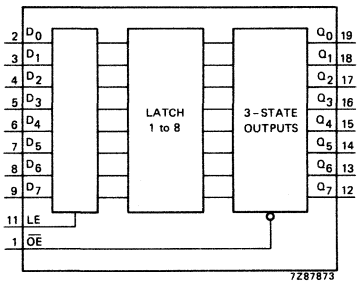
HC/HCT564

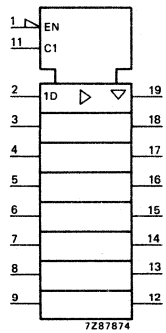




Octal D-type flip-flop; positive-edge trigger; 3-state; inverting

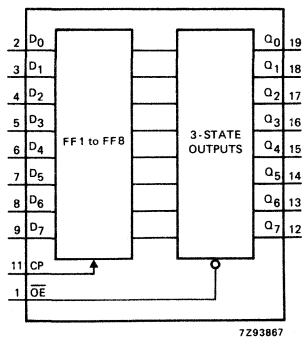
HC/HCT573

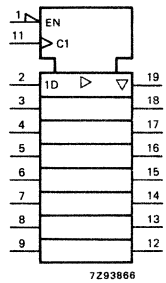




Octal D-type transparent latch; 3-state

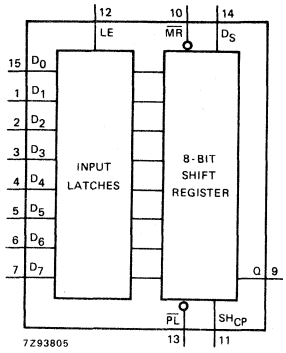
HC/HCT574

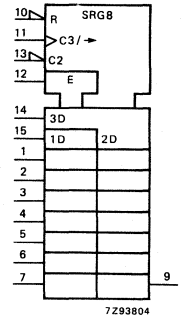




Octal D-type flip-flop; positive-edge trigger; 3-state

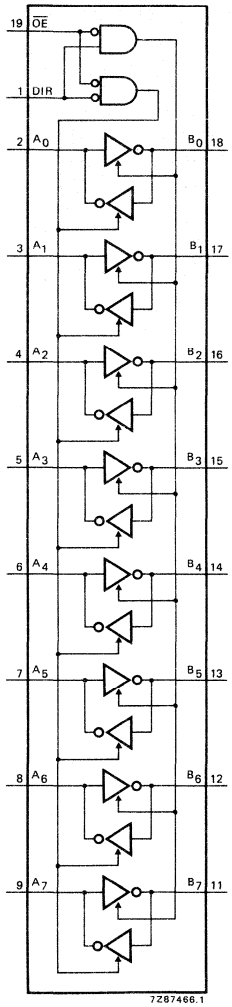
HC/HCT7597

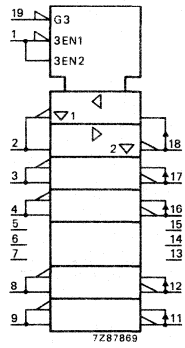




8-bit shift register with input latches

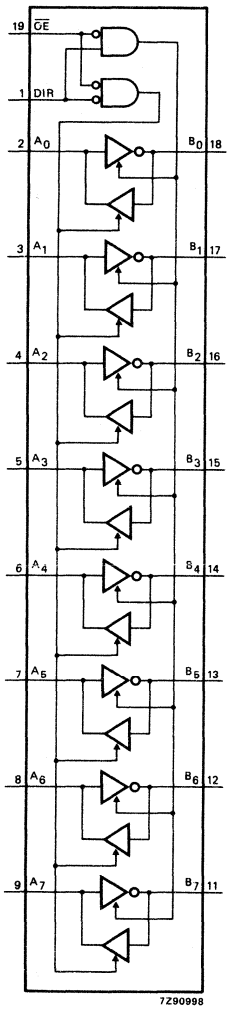
HC/HCT640

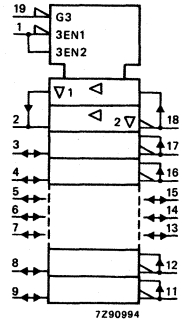




Octal bus transceiver; 3-state; inverting

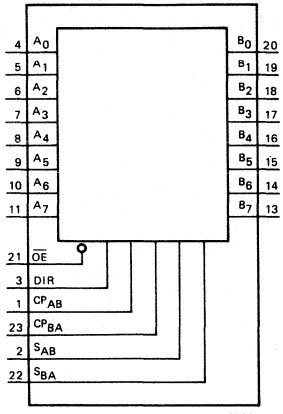
HC/HCT643

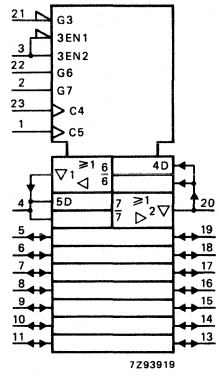




Octal bus transceiver; 3-state; true/inverting

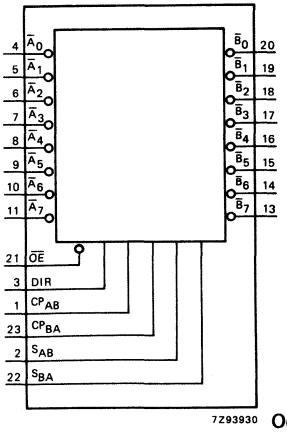
HC/HCT646

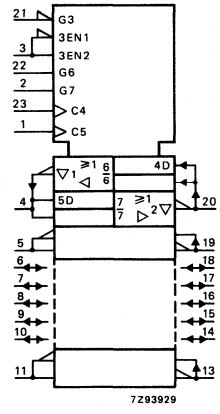




Octal bus transceiver/register; 3-state

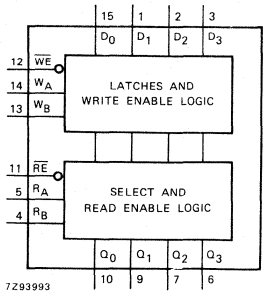
HC/HCT648

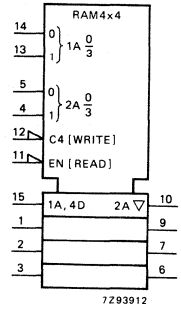




Octal bus transceiver/register; 3-state; inverting

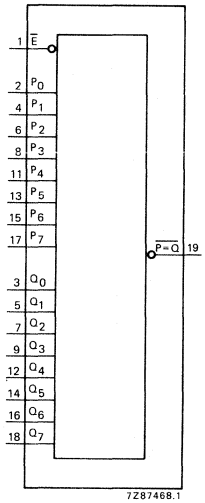
HC/HCT670

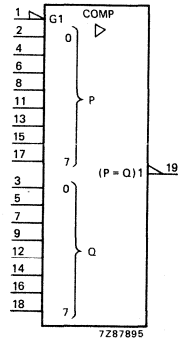




4 x 4 register file; 3-state

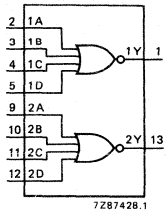
HC/HCT688

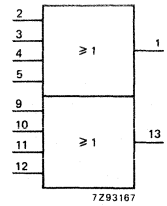




8-bit magnitude comparator

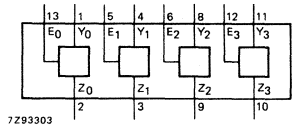
HC/HCT4002

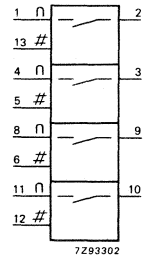




Dual 4-input NOR gate

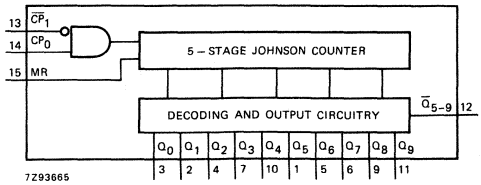
HC/HCT4016

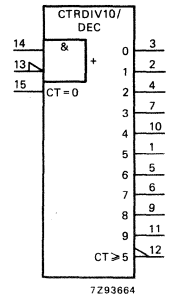




Quad bilateral switches

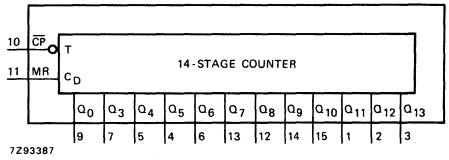
HC/HCT4017

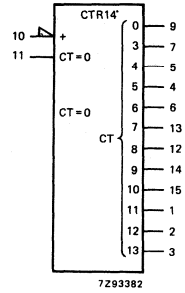




Johnson decade counter with 10 decoded outputs

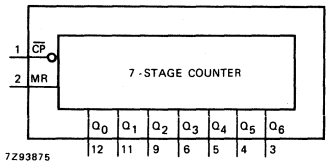
HC/HCT4020

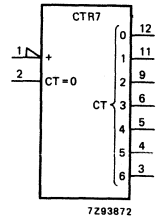




14-stage binary ripple counter

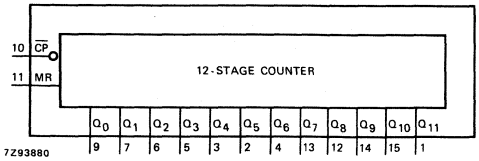
HC/HCT4024

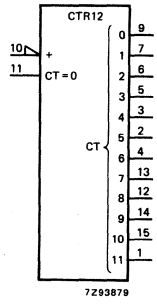




7-state binary ripple counter

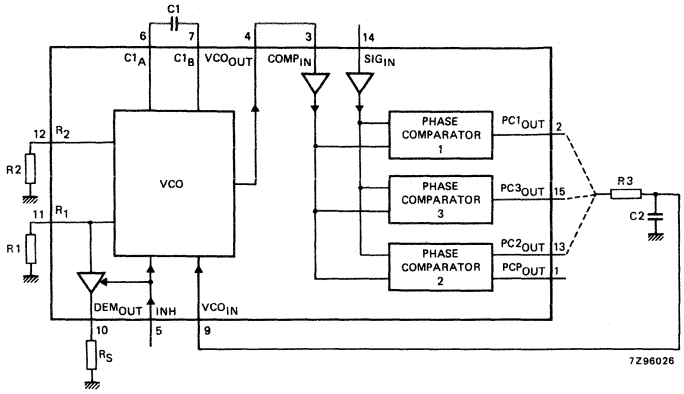
HC/HCT4040

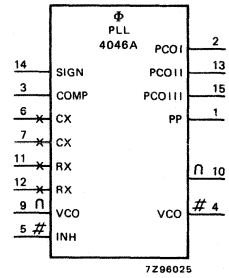




12-stage binary ripple counter

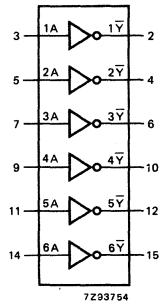
HC/HCT4046A

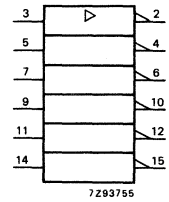




Phase-locked-loop with VCO

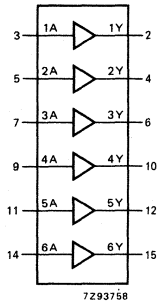
HC4049

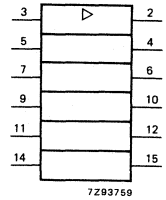




Hex inverting HIGH-to-LOW level shifter

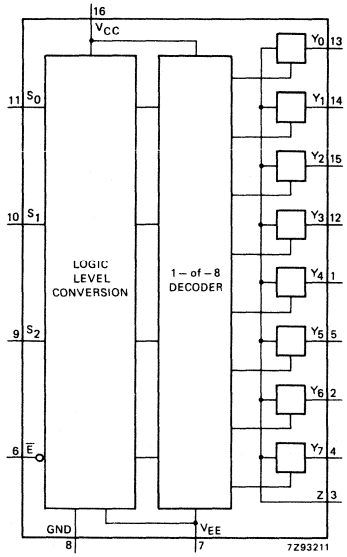
HC4050

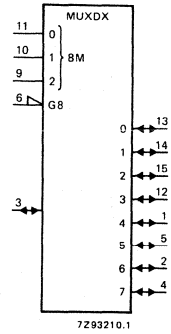




Hex HIGH-to-LOW level shifter

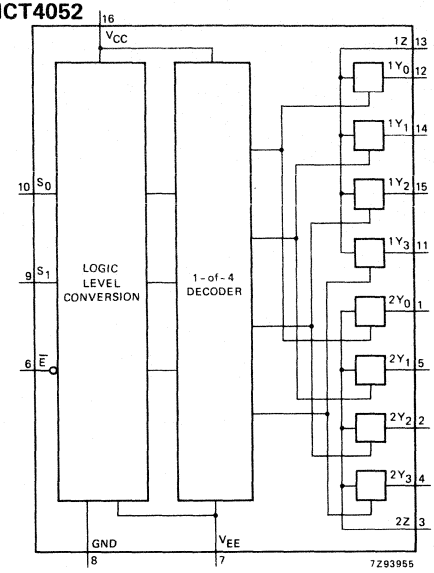
HC/HCT4051

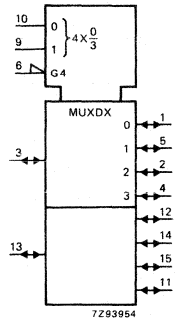




8-channel analog multiplexer/demultiplexer

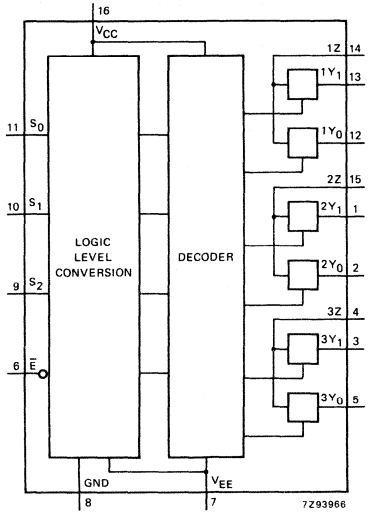
HC/HCT4052

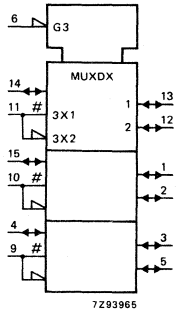




Dual 4-channel analog multiplexer/demultiplexer

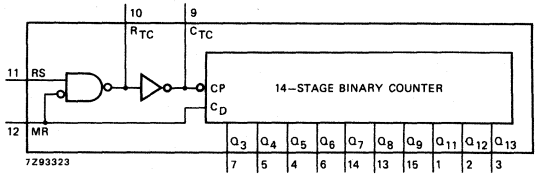
HC/HCT4053

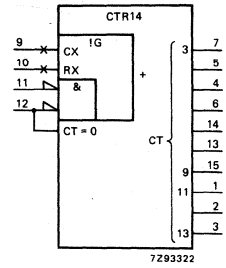




Triple 2-channel analog multiplexer/demultiplexer

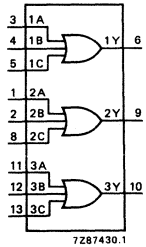
HC/HCT4060

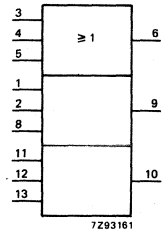




14-stage binary ripple counter with oscillator

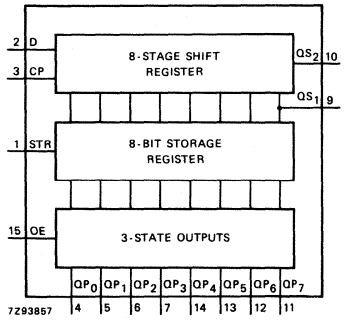
HC/HCT4075

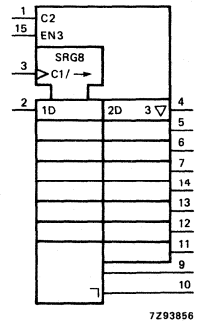




Triple 3-input OR gate

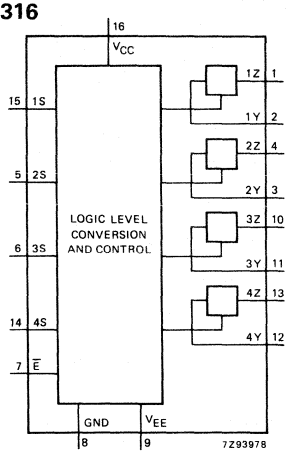
HC/HCT4094

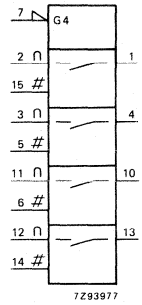




8-stage shift-and-store bus register

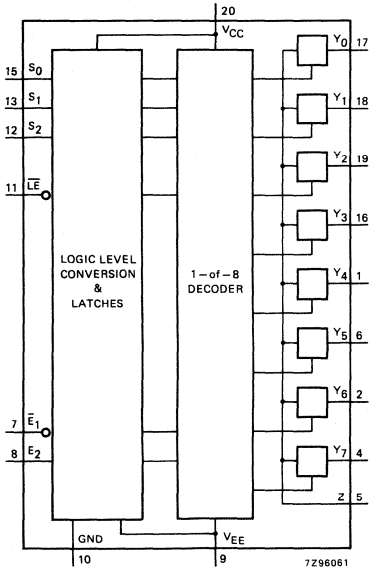
HC/HCT4316





Quad bilateral switches

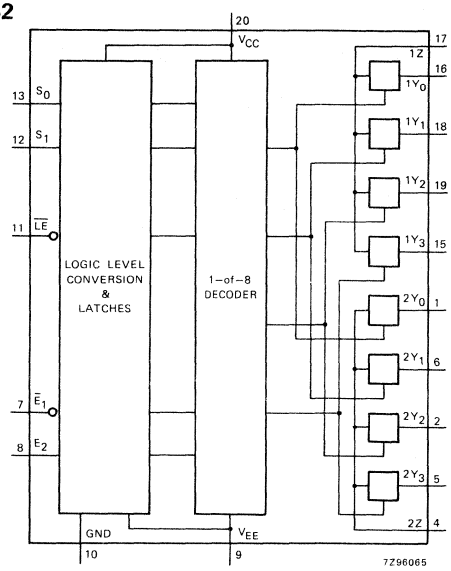
HC/HCT4351



IEC SYMBOL
IN
PROGRESS

8-channel analog multiplexer/demultiplexer with latch

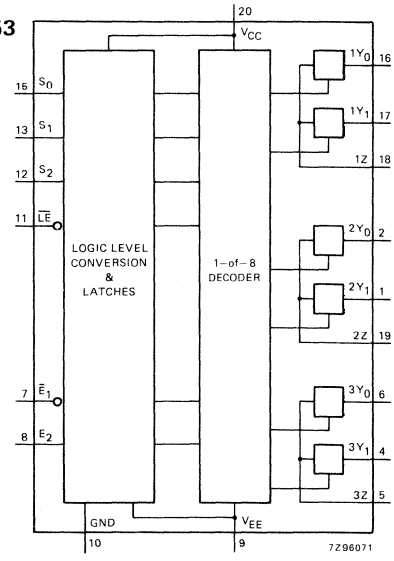
HC/HCT4352



IEC SYMBOL
IN
PROGRESS

Dual 4-channel analog multiplexer/demultiplexer with latch

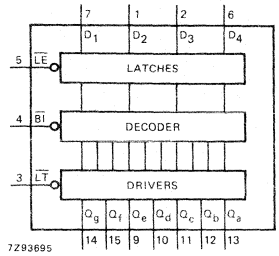
HC/HCT4353

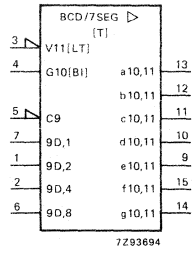


IEC SYMBOL
IN
PROGRESS

Triple 2-channel analog multiplexer/demultiplexer with latch

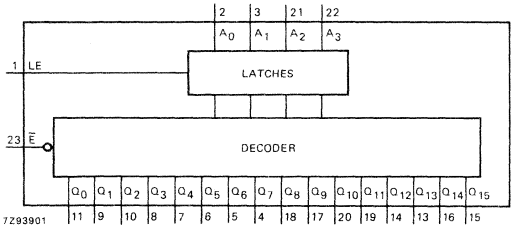
HC/HCT4511

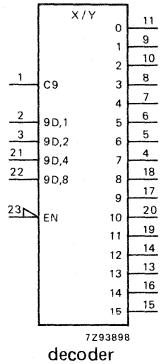




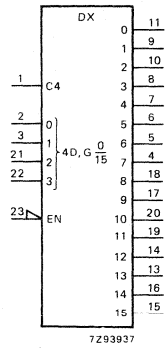
BCD to 7-segment latch/decoder/driver

HC/HCT4514





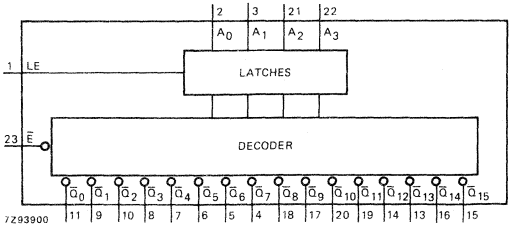
decoder

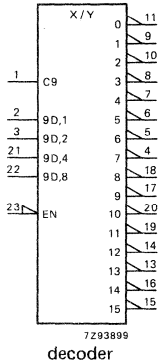


demultiplexer

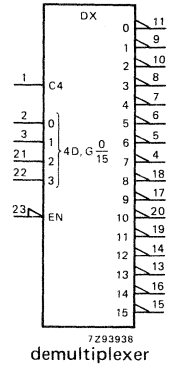
4-to-16 line decoder/demultiplexer with input latches

HC/HCT4515





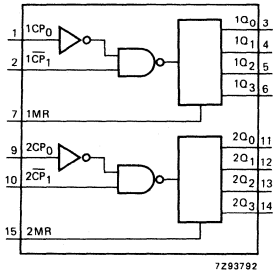
decoder

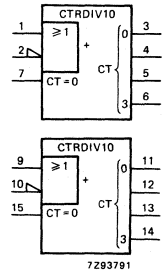


demultiplexer

4-to-16 line decoder/demultiplexer with input latches

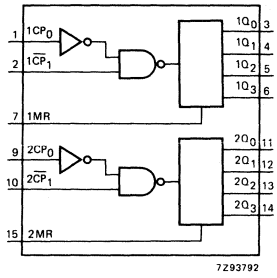
HC/HCT4518

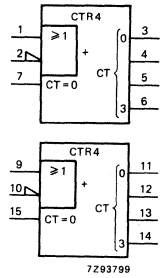




Dual synchronous BCD counter

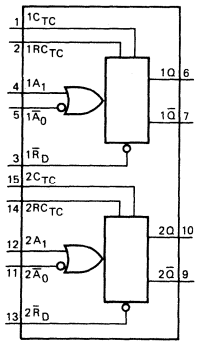
HC/HCT4520

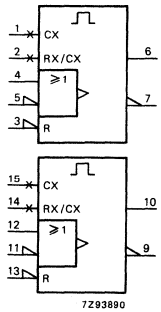




Dual synchronous 4-bit binary counter

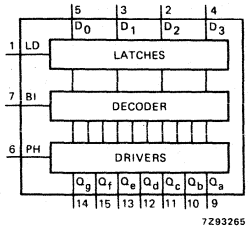
HC/HCT4538

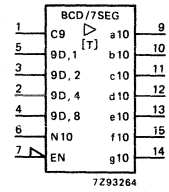




Dual retriggerable precision monostable multivibrator

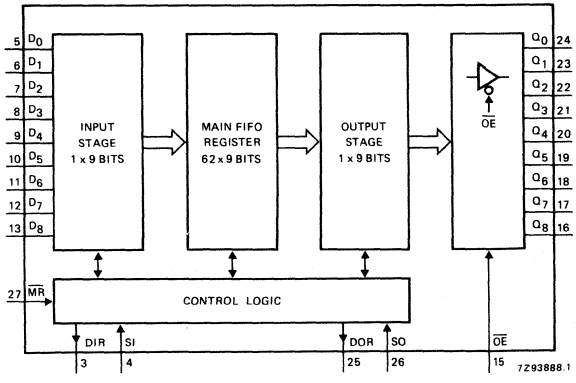
HC/HCT4543





BCD to 7-segment latch/decoder/driver for LCDs

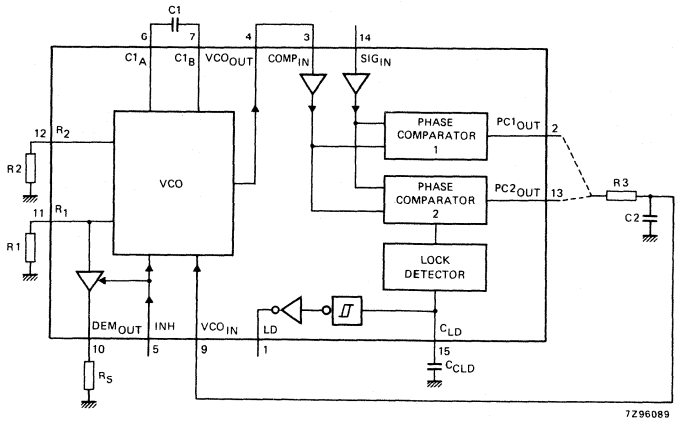
HC/HCT7030

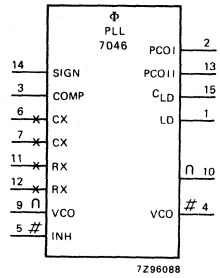


IEC SYMBOL
IN
PROGRESS

9-bit x 64-word FIFO register; 3-state

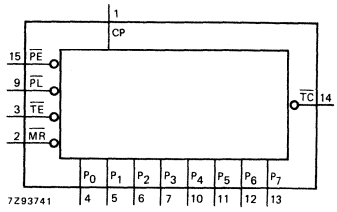
HC/HCT7046A





Phase-locked-loop with lock detector

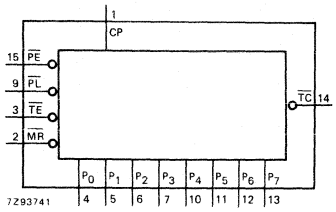
HC/HCT40102



IEC SYMBOL
IN
PROGRESS

8-bit synchronous BCD down counter

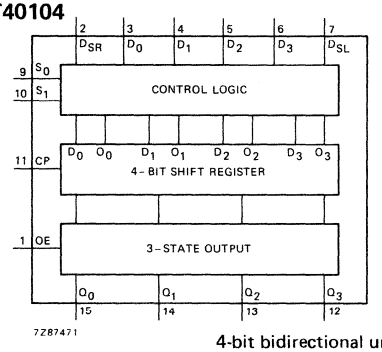
HC/HCT40103

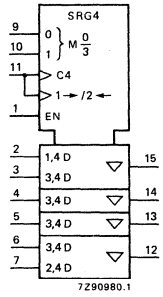


IEC SYMBOL
IN
PROGRESS

8-bit synchronous binary down counter

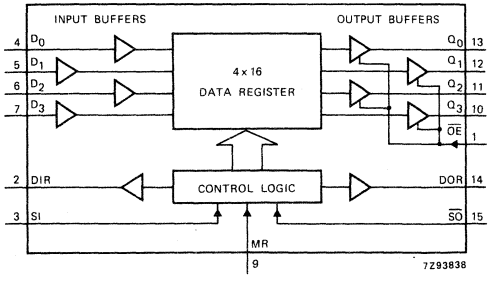
HC/HCT40104





4-bit bidirectional universal shift register; 3-state

HC/HCT40105



IEC SYMBOL
IN
PROGRESS

4-bit x 16-word FIFO register

IEC SYMBOLOGY

SUMMARY OF IEC SYMBOLOGY

INTRODUCTION

The logic symbology used in the HCMOS published data follows the system developed by the International Electrotechnical Commission (IEC). The representation is very effective in that it shows the exact relationship between every input and output of digital circuits without having to detail internal logic. Basic logic functions are represented by symbols; in the symbols for more complex functions, use is made of 'dependency notation' that specified interrelationships of the digital inputs/outputs.

This summary describes the various elements used in symbol construction and the rules and definitions that apply.

SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying-symbols (Fig. 1). The purpose of a general qualifying-symbol is to accurately portray the logic function of the element and those used in this handbook are listed in Table 1. The preferred direction of signal flow through symbols and associated circuit is from left to right; inputs are on the left and outputs on the right. Exceptions to this convention are indicated by arrowheads in the signal lines showing the direction of signal flow, as shown in Fig. 12.

All outputs of a single element of a symbol have internal logic states that are determined by the element's function, unless otherwise indicated by an associated qualifying- symbol.

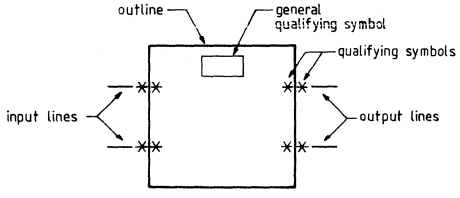


Fig. 1 Symbol composition.

Adjacent elements in a composite symbol may be joined by a common boundary line. When this boundary line is parallel to the direction of signal flow there is no logic connection between the elements, but when the line is perpendicular to the direction of signal flow then there is at least one logic connection between them. The number of logic connections between elements is shown by qualifying- symbols, but if there are no qualifying-symbols on either side of the common line then the elements have just one logic connection.

When a composite symbol contains at least one input common to one or more of the elements, a common-control block can be used. In the example of Fig. 2 the common-control block provides an input to each of the elements below it, this can be otherwise qualified by dependency notation.

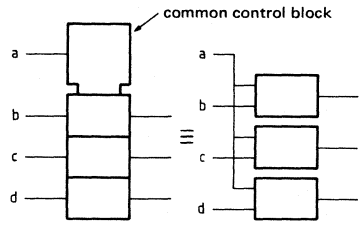


Fig. 2 Common-control block.

An output that depends on all elements of a composite symbol can be shown as an output from a common-output element. This part of the symbol is distinguishable by a double boundary line as shown in Fig. 3. The common-output element may have other inputs. Its function must be indicated by a qualifying-symbol within the outline.

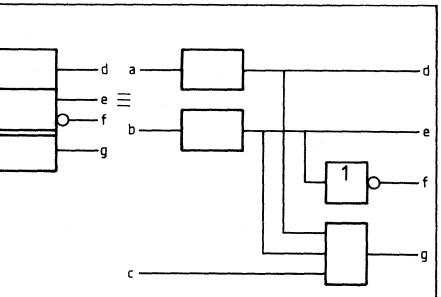


Fig. 3 Common-output element.

QUALIFYING SYMBOLS

General qualifying-symbols

Table 1 shows the general qualifying-symbols used in this publication. These characters are usually placed near the top centre of a symbol element and define the logic function that is represented by the symbol or element.

Table 1 Qualifying-symbols - General

qualifying-symbol	definition
&	AND element. If all inputs are at internal logic "1" then the output is at internal logic "1"
≥m	Logic threshold element. If at least m inputs are at internal logic "1" then the output is at internal logic "1"
≥1	OR element. If at least one input is at internal logic "1" then the output is at internal logic "1"
=m	m-out-of-n element. Given that m < n; if m inputs are at internal logic "1" then the output is at internal logic "1"
=1	EXCLUSIVE-OR element. If only one input is at internal logic "1" then the output is at internal logic "1"
=	Logic identity element. If all inputs have the same logic state then the output is at internal logic "1"
>n/2	Majority element. If the majority of inputs are at internal logic "1" then the output is at internal logic "1"
2k	Even element. If an even number of inputs are at internal logic "1" then the output is at internal logic "1"
2k+1	Odd element. If an odd number of inputs are at internal logic "1" then the output is at internal logic "1"
1	Buffer element without amplified output. If the input is at internal logic "1" then the output is at internal logic "1"
or	Buffer element with amplified output. The triangle points in the direction of signal flow
	Bi-threshold detector. Schmitt-trigger
X/Y	Coder or code converter. X and Y may be replaced by appropriate indications of the codes used
MUX	Multiplexer/ data selector
DX	Demultiplexer
MUXDX	Bidirectional selector
Σ	Adder

qualifying-symbol	definition	
P-Q	Subtractor	
CPG	Look-ahead carry generator	
Π	Multiplier	
COMP	Comparator	
ALU	Arithmetic logic unit	
	Retriggerable monostable element	
1	Non-retriggerable monostable element	
G	Astable element	
!G	Synchronous-starting astable element	
G!	Synchronous-stopping astable element	
SGRm	Shift register. "m" = number of bits	
CTRm	Binary counter. "m" = number of bits or is an indication of the cycle length 2^m	
CTRDIVm	Counter with cycle length m	
ROMm1xm2	Read only memory	m1 is the number of words
PROMm1xm2	Programmable read only memory	
RAMm1xm2	Random access memory	
CAMm1xm2	Associative memory	m2 is the number of bits per word
FIFOm1xm2	First-in/first-out memory	
I=0	Initial logic "0" state. When power is switched ON, the element goes to internal logic "0"	

qualifying-symbol	definition
I = 1	Initial logic "1" state. When power is switched ON, the element goes to internal logic "1"
NV	Non-volatile. The internal logic state is maintained regardless of power ON or OFF
Φ	Very complicated element. Depicted by a 'grey box' symbol. Within the 'grey box' outline, the Φ qualifying-symbol is accompanied by a further qualifying expression, e.g. ERR - for error detector

Qualifying-symbols for inputs and outputs

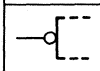
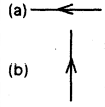
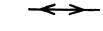
Referring to Table 2, qualifying-symbols for inputs and outputs, the logic negation indicator is used in pure logic diagrams to indicate that an external logic "0" ("1") produces an internal logic "1" ("0") at the input, or that an internal logic "1" ("0") produces an external logic "0" ("1") at the output.

The polarity indicator is used in detailed logic diagrams to indicate which logic level corresponds with the internal logic "1". The following may occur:

- an input or output **with** polarity indicator indicates that the logic level "L" (LOW) corresponds to an internal logic "1".
- an input or output **without** polarity indicator indicates that the logic level "H" (HIGH) corresponds to an internal logic "1".

In an array of elements, if the same general qualifying- symbol and the same qualifying-symbols associated with inputs and outputs should appear inside each element of the array, then they are usually shown only in the first element. Similarly, for large identical elements with subdivisions, the subdivisions may be shown only in the first element. This is done to simplify the array and ease recognition. As an example, omissions of both repeating qualifying-symbols and subdividing lines can be seen in the HC/HCT242 symbol.

Table 2 Qualifying-symbols - Inputs and Outputs

qualifying-symbol	definition of input or output
	Logic negation at an input. An external logic "0" ("1") produces an internal logic "1" ("0")
	Logic negation at an output. An internal logic "1" ("0") produces an external logic "0" ("1")
	Polarity indicator at an input. A logic "L" (LOW) level ("H" (HIGH) level) at an input produces an internal logic "1" at that input
	Polarity indicator at an output. An internal logic "1" ("0") at an output produces a logic "L" (LOW) level ("H" (HIGH) level) at that output
	Polarity indicator at an input where the signal flow is from right to left
	Polarity indicator at an output where the signal flow is from right to left
	(a) Indicator for direction of signal flow: (a) from right to left; (b) from bottom to top. With no indication of direction, flow is left to right or top to bottom
	Bidirectional information flow (alternate)
	Non-logic connection
	Input for analogue signals
	Input for digital signals (used only to avoid confusion)

Symbols inside the outline

Table 3 shows some of the symbols used within the symbol-outlines. Other symbols used in this handbook but not shown here are self-explanatory. Generally these are associated with arithmetic operations but all are in accordance with the IEC system. When non-standard information is shown inside a symbol-outline, it is enclosed in square brackets.

It can be seen in Table 3 that open-collector, open-emitter and three-state outputs have distinctive symbols. Note that an enable input (EN) affects all of the circuit outputs and has no effect on the inputs. When an enable input affects only certain outputs and/or one or more inputs, a form of dependency notation will indicate this (see 'Dependency Notation, EN-dependancy').

Another important point is that a D-input is always the data input of a storage element. An internal logic "1" at the D-input sets the storage element to its "1" state, and an internal logic "0" at the D-input resets the storage element to its "0" state.

Grouping of inputs or outputs is indicated by the bit-grouping symbol. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. The weights of input and output lines are represented by powers-of-two only when the bit-grouping symbol is used, otherwise decimal equivalents are used. Inputs grouped together by this symbol produce an internal number that is the sum of the individual input weights at logic "1". This number can be a number on which a mathematical function is performed, an identifying number used in dependency notation or a value that becomes the content (CT) of the element (see Fig. 29). A frequent use of the bit-grouping symbol is in memory addressing, see also 'Use of Bit-grouping to Produce Affecting Inputs'. For outputs, usage of the bit-grouping symbol is similar to that of inputs; the number produced by the sum of the output weights is the internal number, or the content (CT) produced by the circuit.

The symbols shown in Table 3 may be used to indicate the internal connections between logic elements abutted together. Each logic connection may be shown by qualifying-symbols at one or both sides of the common line, however, if confusion could arise about the number of connections, one of the internal connection symbols may be used.

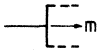
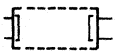
The internal (virtual) input is an input originating somewhere within the circuit and not connected directly to a terminal, and similarly the internal (virtual) output is not connected directly to a terminal.

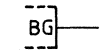
Table 3 Symbols inside the outline

symbol inside outline	explanation
/	Solidus. Separator used in input and output labels. May be interpreted as an OR function
,	Comma. Separator with no logic significance
	Delayed output symbol for pulse and data-lock-out elements. The output change is delayed until the input that initiated the change (e.g. a "C" input) returns to its initial external state or level
	Bi-threshold inputs. Inputs with hysteresis
	Open output with low-impedance "L" (LOW) level
	Passive pull-up output. Similar to open output with low-impedance "L" level but with a built-in passive pull-up
	Open output with low-impedance "H" (HIGH) level

QUALIFYING-SYMBOLS (continued)

Table 3 Symbols inside the outline (continued)

symbol inside outline	explanation
	Passive pull-down output. Similar to open output with low-impedance "H" level but with a built-in passive pull-up
	Three-state output
	Enable input. When at internal logic "1", all outputs are enabled. When at internal logic "0": open outputs are OFF; three-state outputs retain their normal, defined internal logic state but give an external high-impedance state; all other outputs are at internal logic "0"
R, S, C, T	Control inputs of bistable elements
J, K, R, S, D	Information inputs of bistable elements
	Shift input. The direction of shift is to the right or down when the arrow points to the right, or to the left or up when the arrow points to the left. The number may be ommitted when "m" = 1
	
	Counting input. Count-up and count-down are indicated by + and - respectively. The number "m" is the count per command and may be ommitted when "m" = 1
	
	Bit-grouping symbol. "m" is the highest power of 2 in the group
	Content input. The internal logic "1" sets the element to the value "m"
	Content output. "*" is the value of the element that sets the output to an internal logic "1" (e.g. CT = 0, CT ⩾ 5, CT ≠ 4...9)
	Line-grouping symbol. The inputs or outputs enclosed by this symbol form a single logic input or output
	Fixed-mode input. This input is permanently at internal logic "1"

symbol inside outline	explanation
	Fixed-state output. This output is permanently at internal logic "1"
a...g	Seven segments of a display element
	Extension input. Input intended for connection to an extender output
	Extender output. Output to an extension input
	Operand input. This input represents one bit of an operand on which one or more mathematical functions are performed; "m" is the decimal equivalent of the **weight** of the bit. If the **weights** of all Pm inputs of the element are powers of 2 then "m" is the exponent of the power of 2
	Operand input. See Pm
	'Smaller-than' input to a magnitude comparator
	'Greater-than' input to a magnitude comparator
	'Equal' input to a magnitude comparator
	'Borrow-in' input to an arithmetic element
	'Borrow-generate' input to an arithmetic element
	'Borrow-generate' output from an arithmetic element

symbol inside outline	explanation
BO	'Borrow-out' output from an arithmetic element
BP	'Borrow-propagate' input to an arithmetic element
BP	'Borrow-propagate' output from an arithmetic element
CI	'Carry-in' input to an arithmetic element
CG	'Carry-generate' input to an arithmetic element
CG	'Carry-generate' output from an arithmetic element
CO	'Carry-generate' output from an arithmetic element
CP	'Carry-propagate' input to an arithmetic element
CP	'Carry-propagate' output from an arithmetic element
Π	Result of a multiplication
Σ	Result of an addition
P-Q	Result of a subtraction
[··]	Added information

symbol inside outline	explanation
φm	Clock phase. "m" is the clock phase number
CX	Connection for external capacitor(s)
RX	Connection for external resistor(s)
	Dynamic input. A transition from logic "L" level to "H" level produces a transitory internal logic "1"
	Dynamic input. A transition from logic "H" level to "L" level produces a transitory internal logic "1"
	Internal connection. A logic "1" at the left-hand side produces a logic "1" at the right-hand side
	Negated internal connection. A logic "1" at the left-hand side produces a logic "0" at the right-hand side
	Dynamic internal connection. A transition from internal logic "0" to internal logic "1" at the left-hand side produces a transitory logic "1" at the right-hand side
	Negated dynamic internal connection. A transition from internal logic "1" to internal logic "0" at the left-hand side produces a transitory internal logic "1" at the right-hand side
	Internal (virtual) input. This input is always at internal logic "1" state unless this is overridden or modified
	Internal (virtual) output. The effect on the internal input connected to this output must be indicated by dependency notation

DEPENDENCY NOTATION

General conventions of dependency notation

Dependency notation is the powerful tool that makes IEC symbols compact and yet meaningful. With IEC symbols, the relationships between inputs and other inputs, between outputs and other outputs, and between inputs and outputs are clearly illustrated without the necessity to show all elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying-symbols for an element's function.

In dependency notation, the terms "affecting" and "affected" are used. In cases where it is not evident which inputs must be selected as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the most convenient input has been chosen.

The types of dependency described in this section are "G" (AND); "V" (OR); "N" (negate, or EXCLUSIVE-OR); "Z" (interconnection); "C" (control); "S" and "R" (set and reset); "EN" (enable); "M" (mode); and "A" (address).

The general rules applied to dependency notation are:

- the input (or output) affecting other inputs or outputs is labelled with the letter symbol that indicates the relationship involved (e.g. G for AND) followed by an appropriately-chosen identifying number; and
- each input or output affected by that affecting input (or output) is labelled with that same number.

If two affecting inputs or outputs have the same letter and the same identifying number, they are ORed together (see Fig. 4).

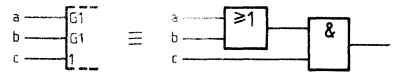


Fig. 4 ORed affecting inputs.

If an input or output is affected by more than one affecting input, each identifying number separated by a comma will appear in the label of the affected one. The normal reading order of these numbers is the same as the sequence of the affecting relationships (see Fig. 5).

Fig. 5 Input affected by more than one input.

If the labels denoting the function of affected inputs or outputs are numbers, (e.g., outputs of a coder), the identifying number of both affecting inputs and affected inputs or outputs is replaced by another character selected to avoid ambiguity, e.g., Greek letters (see Fig. 6).

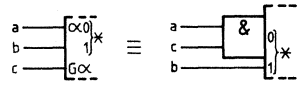


Fig. 6 Substitution for numbers.

If it is the complement of the input's (or output's) internal logic state that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (see Fig. 7).

If the affected input or output has a label to denote its function (e.g. "D"), this label will have the identifying number of the affecting input as a prefix (see Fig. 13).

G-dependency

The traditional method of showing an AND relationship was to use an explicit drawing of an AND gate with the signals connected to the inputs of the gate. With IEC symbology (see Fig. 7), input "b" and input "a" are ANDed together and the complement of "b" is ANDed with "c". The letter G has been chosen to indicate AND relationships and is placed at input "b", within the outline. A number considered appropriate by the designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input "c".

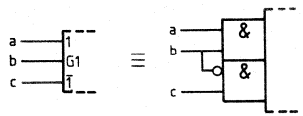


Fig. 7 G-dependency between inputs.

In Fig. 8, output "b" affects input "a" with an AND relationship. The lower example shows it is the internal logic state of "b", unaffected by the negation sign, that is ANDed.

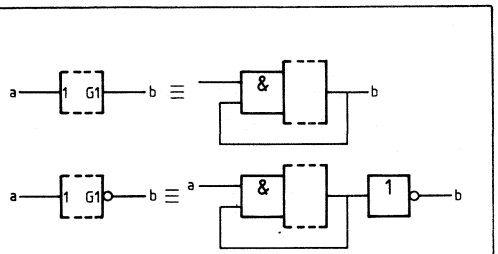


Fig. 8 G-dependency between outputs and inputs.

In Fig. 9, input "a" is ANDed with the dynamic input "b".

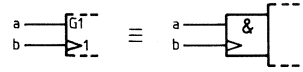


Fig. 9 G-dependency with a dynamic input.

To summarize G-dependancy using input G and allotted number m: when a Gm-input (Gm-output) is at internal logic "1", all inputs and outputs affected by Gm will be at their normally defined internal logic states. When the Gm-input (Gm-output) is at internal logic "0", all inputs and outputs affected will be at internal logic "0".

V-dependency

When a Vm-input (Vm-output) is at internal logic "1", all inputs and outputs affected by Vm will be at internal logic "1". When the Vm-input (Vm-output) is at internal logic "0", all inputs and outputs affected by Vm will be at their normally defined internal logic states (see Fig. 10).

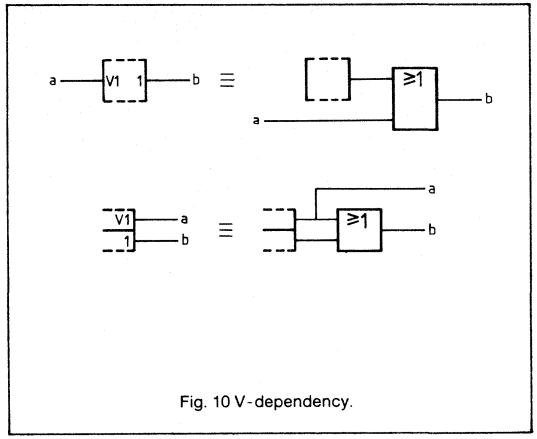


Fig. 10 V-dependency.

N-dependency

Each input or output affected by an Nm-input (or output) is EXCLUSIVE-ORed with the Nm-input (or output) (see Fig. 11).

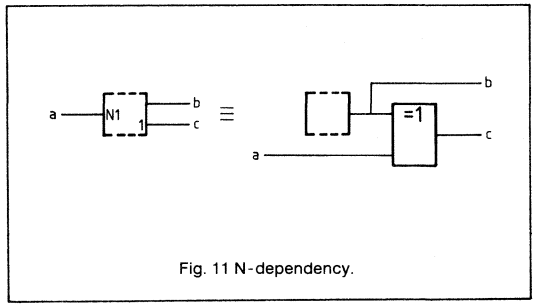


Fig. 11 N-dependency.

When an Nm-input (Nm-output) is at internal logic "1", the internal logic state of each input and each output affected by Nm will be complemented. When an Nm-input (Nm-output) is at internal logic "0", all inputs and outputs affected by Nm will be at their normally defined internal logic states.

DEPENDENCY NOTATION (continued)

Z-dependency

Interconnection dependency is used to indicate internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

All inputs or outputs affected by a Zm-input (or output) will take on the same internal logic state as the Zm-input (or output), unless modified by additional dependency notation (see Fig. 12).

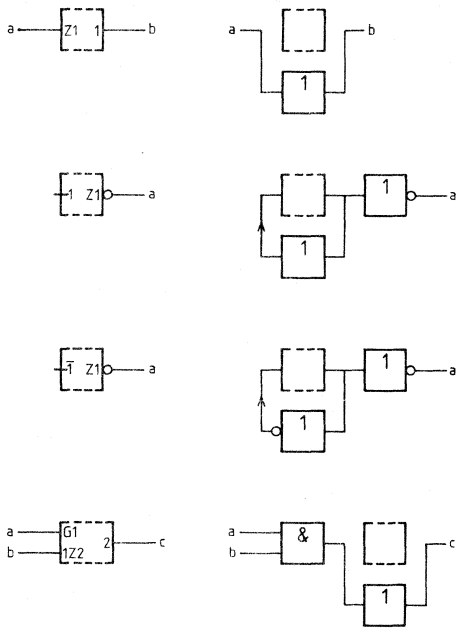


Fig. 12 Z-dependency.

C-dependency

Control inputs enable or disable the data (D, J, K, R or S) inputs of storage elements (see Fig. 13).

When a Cm-input is at internal logic "1", the inputs affected by Cm have their normal effect on the function of the element, i.e. these inputs are enabled. When a Cm-input is at internal logic "0", the inputs affected by Cm are disabled and have no effect on the function of the element.

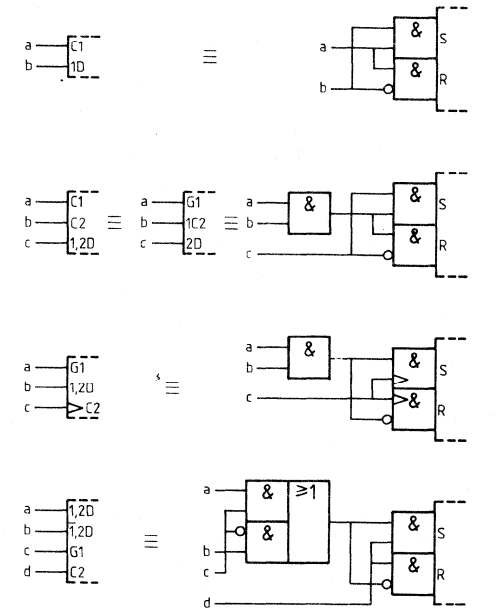


Fig. 13 C-dependency.

EN-dependency

An ENm-input has the same effect on outputs as an EN-input (see Table 1) but it affects both inputs and outputs that have the identifying number "m", whereas an EN-input affects all outputs and no inputs.

The effect of an ENm- input on an affected input is identical to that of a Cm- input (see Fig. 14).

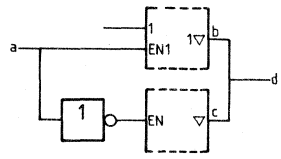


Fig. 14 EN-dependency.

When an ENm-input is at internal logic "1", inputs and outputs affected by ENm are enabled.

When an ENm-input is at internal logic "0": inputs and outputs affected by ENm are disabled; open outputs are turned OFF; passive pull-up outputs will be high-impedance "L" level; passive pull-down outputs will be high-impedance "H" level; 3-state outputs will have their normally defined internal logic states but externally exhibit high-impedance; and all other outputs (e.g., totem-pole outputs) will be at internal logic "0".

S and R-dependencies

Set and reset dependencies are used if the effect of the combination R = S = 1 on a bistable element must be specified. Figure 15a does not use S or R-dependency (? = not specified).

When an Sm-input is at internal logic "1", outputs affected by the Sm-input will react, regardless of the state of an R-input, as they would normally react to the combination S = 1, R = 0 (see Fig. 15b).

When an Rm-input is at internal logic "1", outputs affected by the Rm-input will react, regardless of the state of an S-input, as they would normally react to the combination S = 0, R = 1 (see Fig. 15c).

The non-complementary output patterns in Figs 15d and 15e are only pseudo-stable. The simultaneous return of the inputs to S = R = 0 produces an unforeseeable stable and complementary output pattern.

When an Sm or Rm input is an internal logic "0", it has no effect.

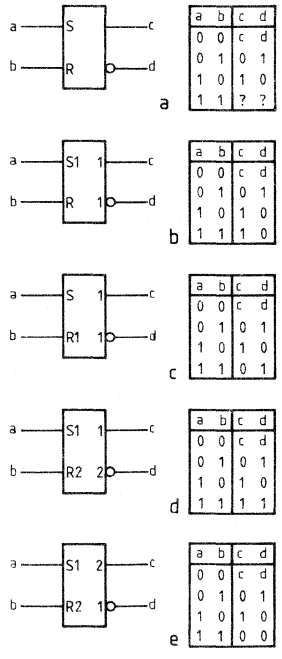


Fig. 15 S and R-dependencies.

M-dependency

Mode dependency indicates that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

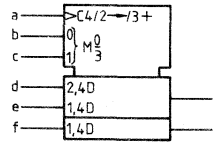
If an input or output has the same affect in different modes of operation, the identifying numbers of the relevant affecting Mm-inputs will appear in parentheses, separated by solidi, in the label of that affecting input or output (see Fig. 20).

M-dependency affecting inputs

When an Mm-input (Mm-output) is at internal logic "1", the inputs affected by this Mm-input (Mm-output) will be enabled.

When an Mm-input (Mm-output) is at internal logic "0", the inputs affected by this Mm-input (Mm-output) will be dis- abled. When an affecting input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the Mm-input (Mm-output) appears has no effect and is to be ignored. This represents the disabling of some of the functions of a multi-function input.

The circuit in Fig. 16 has two inputs, "b" and "c", these control the one of four modes (0, 1, 2 or 3) that will exist at any time. Inputs "d", "e", and "f" are D-inputs subject to dynamic control (clocking) by the "a" input. The numbers 1 and 2 identify the operating modes, and so inputs "e" and "f" are only enabled in mode 1 (for parallel loading) and input "d" is only enabled in mode 2 (for serial loading). Input "a" has three functions: it is the clock for entering data; in mode 2 it causes right-shifting of data (shifts away from the control block); and in mode 3, it causes the contents of the register to be incremented by one.



All operations are synchronous.

Mode 0 (b = 0; c = 0):
The outputs remain at their existing states as the inputs have no effect.

Mode 1 (b = 1, c = 0):
Parallel loading takes place through inputs "e" and "f".

Mode 2 (b = 0, c = 1):
Shifting down and serial loading takes place through input "d".

Mode 3 (b = c = 1):
Counting up takes place in increments of 1 per clock pulse.

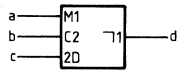
Fig. 16 M-dependency affecting inputs.

DEPENDENCY NOTATION (continued)

M-dependency affecting outputs

When an Mm-input (Mm-output) is at internal logic "1", the affected outputs will be enabled.

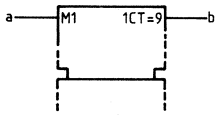
When an Mm-input (Mm-output) is at internal logic "0", the affected outputs will be disabled. When an input or output has several different sets of labels separated by solidi (e.g., 2,4/3,5), any set in which the identifing number of the Mm-input (Mm-output) appears is to be ignored.



Mode 1 (a = 1):
The delayed output symbol is effective only in mode 1 and therefore the device functions as a pulse-triggered D-element.

Mode 2 (a = 0):
The delayed output symbol has no effect and therefore the device functions as a transparent latch.

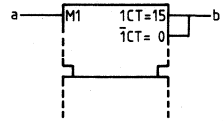
Fig. 17 Flip-flop type determined by mode.



Mode 1 (a = 1):
Output "b" will be an internal logic "1" only when the register content equals 9.

Mode 2 (a = 0):
Since output "b" is located in the common-control block with no defined function outside of mode 1, this output will be an internal logic "0" when input "a" is an internal logic "0", regardless of the register content.

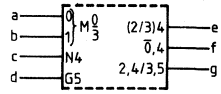
Fig. 18 Disabling an output of the common-control block.



Mode 1 (a = 1):
Output "b" will be an internal logic "1" only when the register content equals 15.

Mode 2 (a = 0):
Input "a" is an internal logic "0", output "b" will be an internal logic "1" only when the register content equals 0.

Fig. 19 Determining an output's function.



Inputs "a" and "b" are binary weighted to generate the numbers 0, 1, 2 or 3 to determine which of the four modes exist.

Mode 0 (a = 0, b = 0):
Since no output label contains a "0", the outputs have their normally defined internal logic states. Output "f" carries a "$\overline{0}$" in its label and this means that output "f" is effected by all modes **except** mode 0.

Mode 1 (a = 1, b = 0):
Only output "f" is affected by mode 1 and is also affected by input "c" (N4).

Mode 2 (a = 0, b = 1):
The outputs "e" and "g" are affected in this mode. They are also affected by input "c" (N4) which means that the internal logic state of the output will be negated at N4 = 1. Output "f" is affected since M0 stands at its internal "0" state. In addition, output "f" is affected by input "c" (N4).

Mode 3 (a = 1, b = 1):
All outputs shown are affected in this mode, with outputs "e" and "f" also affected by input "c" (N4) and input "d" also affecting output "g".

Fig. 20 Dependent relationships affected by mode.

A-dependency

Using address-dependency gives a clear representation of elements, particularly memories, that use address control inputs to select sections of a multi-dimensional array. Such a section of a memory array is usually called a word. Address-dependency allows a symbolic representation of an entire array. An array input at a particular element of a general section is common to the corresponding elements of all selected sections of the array. An array output at a particular element of a general section is the result of ORing the outputs of the corresponding elements of selected sections. If the label of an array output at a particular element of a general section indicates that this output is an open-circuit or a 3-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any input have their normal effect on all sections of the array, whereas inputs affected by an address input only have their normal effect on the section selected by that address input.

An affecting address input has the label "A" followed by an identifying number which corresponds to the address of the particular section of the array selected by this input. Within the general section represented by the symbol, inputs and outputs affected by an "Am" input have the label "A", which stands for the identifying numbers, i.e. the addresses of the particular sections.

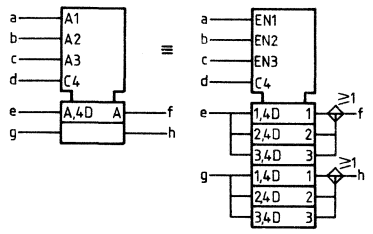


Fig. 21 A-dependency.

Figure 21 shows a 3-word x 2-bit memory having a separate address line for each word; EN-dependency is used to explain the operation. To select word 1, input "a" is forced to logic "1", entering mode 1. Data can now be clocked into the inputs marked "1,4D". Data cannot be clocked into the inputs marked "2,4D" and "3,4D" unless words 2 and 3 are selected. The outputs will be the OR function of the selected outputs, i.e. only those enabled by the active EN functions.

The identifying numbers of affecting inputs correspond to the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, ..), because in the general section represented by the symbol they are replaced by the letter "A".

If there are several sets of affecting "Am" inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter "A" is modified to 1A, 2A, ... These sets of "A" inputs may have the same identifying numbers.

Another illustration of the concept is shown in Fig. 22.

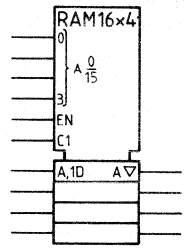


Fig. 22 Array of 15 sections of four transparent latches with 3-state outputs comprising a 16-word x 4-bit random-access memory.

Table 4 Summary of dependency notation

type of dependency	letter-symbol*	affecting input at logic "1"	affecting input at logic "0"
address	A	permits action (address selected)	prevents action (address not selected)
control	C	permits action	prevents action
enable	EN	permits action	prevents action of inputs; open outputs OFF; ▽ outputs at external high impedance, no change in internal logic state; ⬙ outputs high impedance "H" level; ⬘ outputs high impedance "L" level; other outputs at internal "0" state
AND	G	permits action	imposes "0" state
mode	M	permits action (mode selected)	prevents action (mode not selected)
negate (EXCLUSIVE OR)	N	complements state	no effect
reset	R	affected output reacts as it would to S = "0", R = "1"	no effect
set	S	affected output reacts as it would to S = "1", R = "0"	no effect

DEPENDENCY NOTATION (continued)

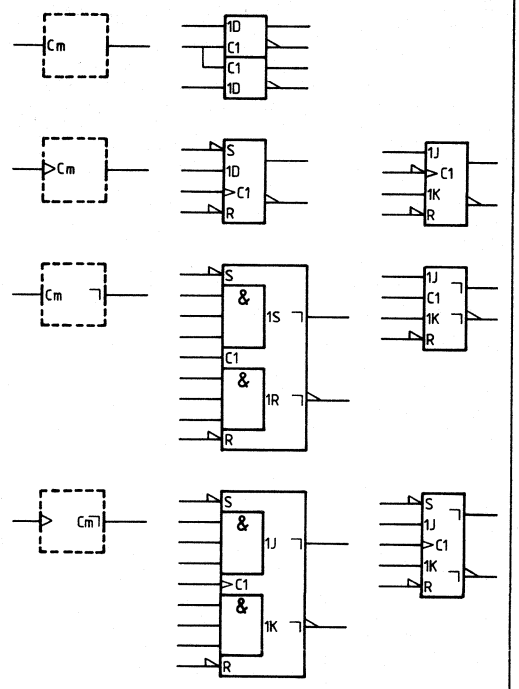
A-dependency (continued)

type of dependency	letter-symbol*	affecting input at logic "1"	affecting input at logic "0"
OR	V	imposes "1" state	permits action
inter-connection	Z	imposes "1" state	permits action

* These letter symbols appear at the **affecting** input (or output) and are followed by a number. Each input (or output) **affected** by that input is labelled with that same number. The descriptions do not apply when the labels "EN", "R" and "S" appear at inputs without numbers following; the action of these inputs is described in 'Symbols inside the outline'.

BISTABLE ELEMENTS

The dynamic input symbol, the delayed output symbol and dependency notation allow the four main types of bistable elements to be shown and make synchronous and asynchronous inputs easily recognizable (see Fig. 23). A fifth type of bistable, the direct acting "SR" element, is mentioned in 'S and R-dependencies'.



The left-hand column of drawings shows essential distinguishing features of the bistables; the other columns show examples.

Fig. 23 Four types of bistable circuits.

Transparent latches have a level-operated control input. The D-input is active as long as the C-input is at internal logic "1". The outputs respond immediately. Edge-triggered elements accept data from "D", "J", "K", "R" or "S" inputs on the active transition of "C". Pulse-triggered elements require the data to be set up before the start of the control pulse; the "C" input is considered static since the data must be maintained as long as "C" is at logic "1". The output is delayed until "C" returns to logic "0". The data- lock-out element is similar to the pulse-triggered version except that the "C" input is considered to be dynamic, in that shortly after "C" goes through its active transition, the data inputs are disabled and data does not have to be maintained. However the output is still delayed until the "C" input returns to its initial external level.

Note that synchronous inputs can be recognized easily because of labels (1D, 1J, 1K, 1S, 2R) unlike the asynchronous inputs "S", "R", which are not dependent on the "C" inputs.

CODERS

The general symbol for a coder or code-converter is shown in Fig. 24. The labels "X" and "Y" may be replaced by appropriate indications of the code that is used to represent the information at the respective inputs and outputs.

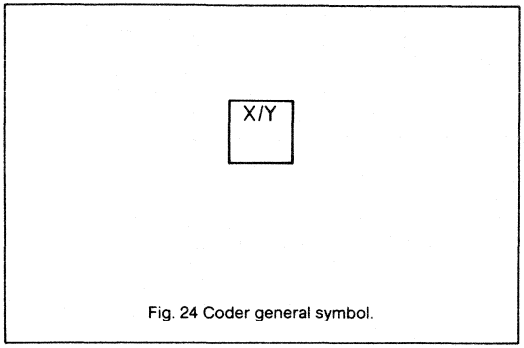


Fig. 24 Coder general symbol.

Indication of code conversion is based on the following rule:

Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

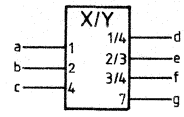
The relationship between the internal logic states of the inputs and the internal value is indicated by:

Labelling the inputs with numbers so that the internal value equals the sum of the weights associated with those inputs that are at internal logic "1"; or by replacing "X" by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationship between the internal value and the internal logic states of the outputs is indicated by:

Labelling each output with a list of numbers representing those internal values that force that output to an internal logic "1". The numbers are separated by solidi (see Fig. 25). This labelling may also be applied when "Y" is replaced by a letter denoting a type of dependency (see 'Use of a coder to produce affecting inputs'). If a continuous range of internal values produces the internal logic "1" at an output, this is indicated by the numbers that begin and end the range, separated by three dots, e.g. "4...9" equals "4/5/6/7/8/9"; or by replacing "Y" with an appropriate indication of the output code and labelling the outputs with characters that refer to this code (see Fig. 26).

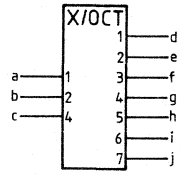
Alternatively the general symbol may be used together with an appropriate reference to a table detailing the relationship between the inputs and outputs. This is a recommended way to symbolize a ROM, or a PROM after it has been programmed.



TRUTH TABLE

inputs			outputs			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Fig. 25 An X/Y code converter.



TRUTH TABLE

inputs			outputs						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

Fig. 26 An X/octal code converter.

USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case the symbols for a coder can be used as an embedded symbol (see Fig. 27).

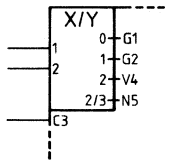


Fig. 27 Producing various types of dependencies.

If all affecting inputs produced by a coder are the same type and their identifying numbers correspond with the numbers shown at the coder outputs, "Y" (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. In this case, affecting input indications should be omitted (see Fig. 28).

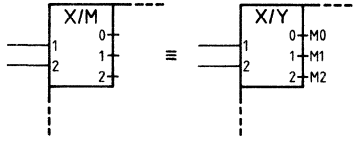


Fig. 28 Producing one type of dependency.

USE OF BIT-GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are the same type and have consecutive identifying numbers (not necessarily corresponding to the numbers that would have been shown at the outputs of the coder) the bit-grouping symbol can be used (see Table 1). Effectively, "k" external lines generate 2^k internal inputs. The bracket precedes the letter denoting the type of dependency which is followed by $^{m1}/_{m2}$. The "m1" is then replaced by the smallest identifying number and "m2" by the largest (see Fig. 29).

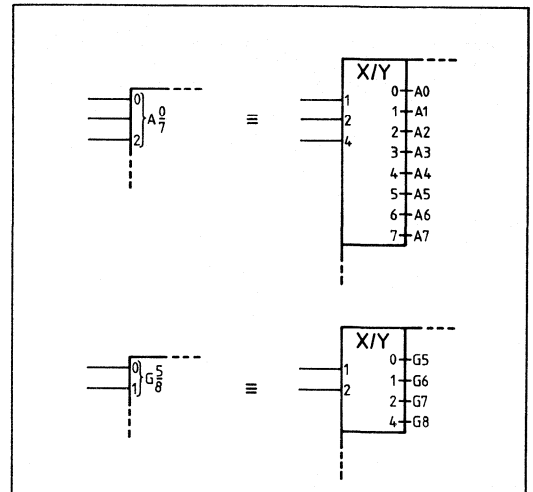


Fig. 29 Use of the bit-grouping symbol.

SEQUENCE OF INPUT LABELS

If an input having a single function is affected by other inputs, the qualifying-symbol (if there is one) for that function is preceded by the labels of the affecting inputs. The left-to-right order of these labels is the sequence in which the effects or modifications must be applied. The affected input has no effect on the element if the logic state of any of the affecting inputs (regardless of the logic states of other affecting inputs) would cause the affected input to have no effect.

If an input has several functions or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of representation is undesirable. In these cases, the input may be shown once with the different sets of labels separated by solidi (see Fig. 30). No meaning is attached to the order of these sets of labels. If one of the functions of an input is as an unlabelled input to an element, a solidus will precede the first set of labels.

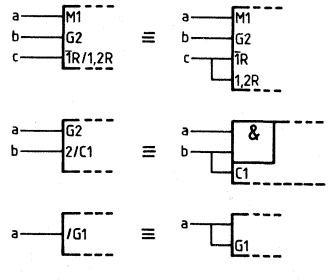


Fig. 30 Input labels.

If all inputs of a combinative element are disabled (have no effect on the function of the element), the internal logic states of the element outputs are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

Labels may be factorized using algebraic techniques (see Fig. 31).

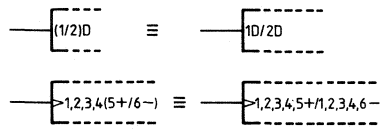


Fig. 31 Factorizing input labels.

When at latched inputs the algebraic factorizing technique is combined with the use of the bit-grouping symbol, the indication "mD" may be placed behind the bit-grouping symbol provided that the proper order of all the other labels is maintained (see Fig. 32).

In "mD", the "m" stands for the identifying numbers of the affecting inputs.

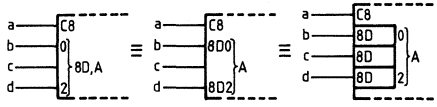


Fig. 32 Algebraic factorizing technique combined with the bit-grouping symbol at "D" inputs.

SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether or not they are identifying numbers of affecting inputs or outputs, these labels are shown in the following order (see Fig. 33):

the delayed output symbol comes first (if to be shown) preceded if necessary by the indications of the inputs to which it must be applied;

followed by the labels indicating modifications to the internal logic state of the output, such that the left-to-right order of these labels is the sequence in which their effects must be applied;

followed by the label indicating the effect of the output on the inputs and other outputs of the element.

Symbols for open-circuit or 3-state outputs, where applicable, are placed just inside boundary of the element adjacent to the output line.

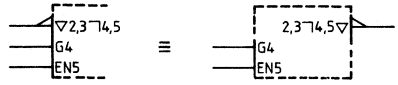


Fig. 33 Placement of 3-state symbols and delayed output symbols.

If an output needs several sets of labels to represent alternative functions, depending on the mode of action, these sets may be shown on different output lines connected together outside the outline. However, there are cases in which this representation is undesirable. In these cases the output may be shown once with the different sets of labels separated by solidi (see Fig. 34).

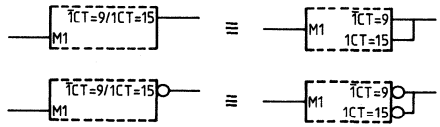


Fig. 34 Output labels.

SEQUENCE OF OUTPUT LABELS (continued)

Adjacent identifying numbers of affecting inputs that are not separated by a non-numeric character are separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting "Mm" input at internal logic "0", this set of labels has no effect on the output.

Labels may be factorized using algebraic techniques (see Fig. 35).

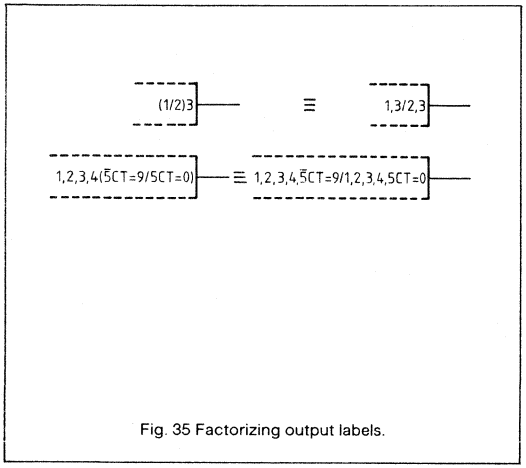


Fig. 35 Factorizing output labels.

If the bit-grouping symbol for outputs is used and the sets of labels of all outputs grouped together differ only in the indications of the weights, the sets of labels may be shown only once between the symbol replacing "*" and the grouping symbol (see Table 3) provided that, except for the grouping symbol and the weights, the proper order of the labels is maintained (see Fig. 36). These sets of labels, therefore, include the symbols for open-circuit, passive pull-down, passive pull-up and 3-state outputs but exclude the indications of weights.

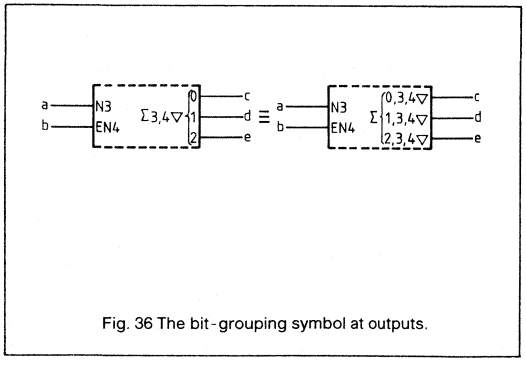


Fig. 36 The bit-grouping symbol at outputs.

RULES FOR SIMPLIFICATION OF SYMBOLS

INTRODUCTION

The IEC symbology can depict a complete integrated circuit but, in many applications, not all available functions are used. For these applications the complete symbol need not be shown and a considerable simplification can be made. To maintain clarity, rules for the simplification of symbols are described in this section.

RULE 1

For an integrated circuit where not all functions are used, the diagram may contain:

a. the complete symbol with indications of which pins are connected to a certain voltage level;

b. a simplified symbol where only the functions used are depicted; the unused pins are detailed in a table including information on whether these pins may remain open (floating) or are to be connected to a certain voltage level.

RULE 2

When two or more pins are shown with a single line, then a comma between the pin numbers means that these pins are connected together; when the pin numbers are separated by a solidus, this means they are separate functions.

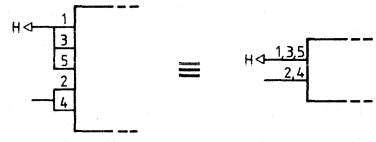


Fig. 38 Example of Rule 2.

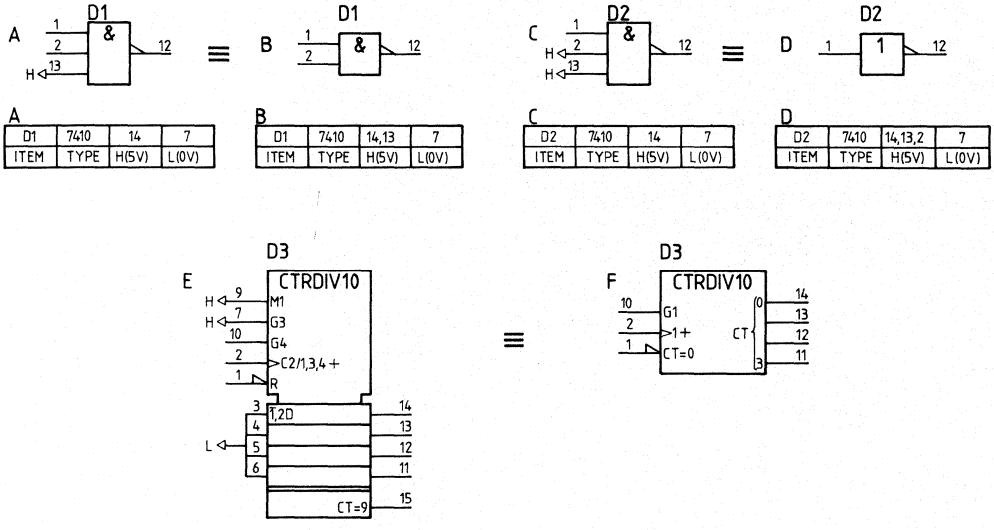


Fig. 37 Examples of Rule 1.

RULE 3

The rules for sets of labels at inputs and outputs using solidi to separate the various parts of a label may be applied when drawing two or more pins with a single line, so the labels must also be joined.

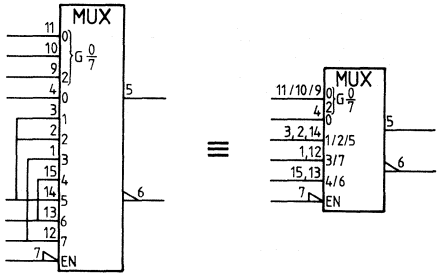


Fig. 39 Example of Rule 3 showing "74151" 8-input multiplexer.

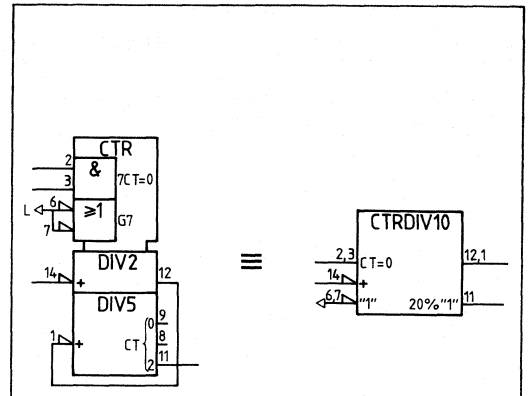


Fig. 41 Example of Rule 4 using TTL "7490".

RULE 4

An output can be connected to an input of equal polarity as shown in Fig. 40C. If the polarity is different this method does not give sufficient information and the methods of Fig.40A or B are then adopted.

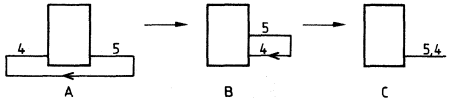


Fig. 40 Examples of Rule 4.

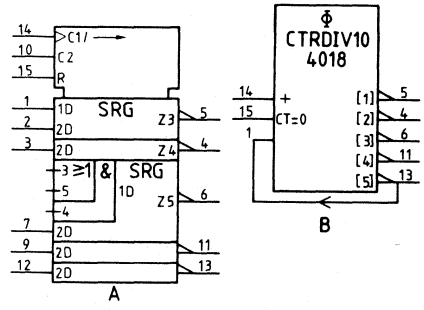


Fig. 42 Example of Rule 4 using CMOS "4018"; the full symbol shown in (A) can be reduced to that of (B) when no parallel loading is applied and the device is used as a divide-by-10 circuit.

RULE 5

Combining elements together to form one element is allowed only if all pin numbers can be shown.

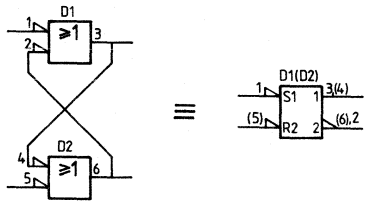


Fig. 43 Example of Rule 5; the pin numbers between parentheses indicate that these belong to another circuit.

RULE 6

A circuit consisting of a combination of two or more elements that appear repeatedly on a diagram, may be replaced by a single symbol. This symbol is used on the diagram, while the complete circuit is shown in an auxiliary diagram elsewhere on the drawing.

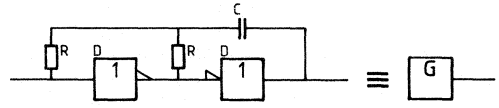


Fig. 44 Example of Rule 6.

RULE 7

A multiple symbol may also be applied for logic symbols.

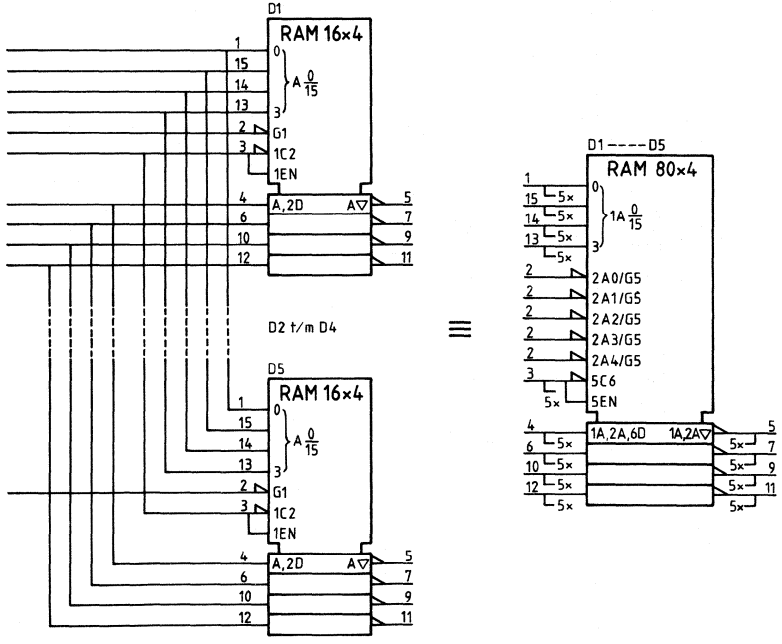


Fig. 45 Example of a multiple symbol showing five TTL "74189" 16x4-bit RAMs connected to enlarge the number of words.

RULE 7 (continued)

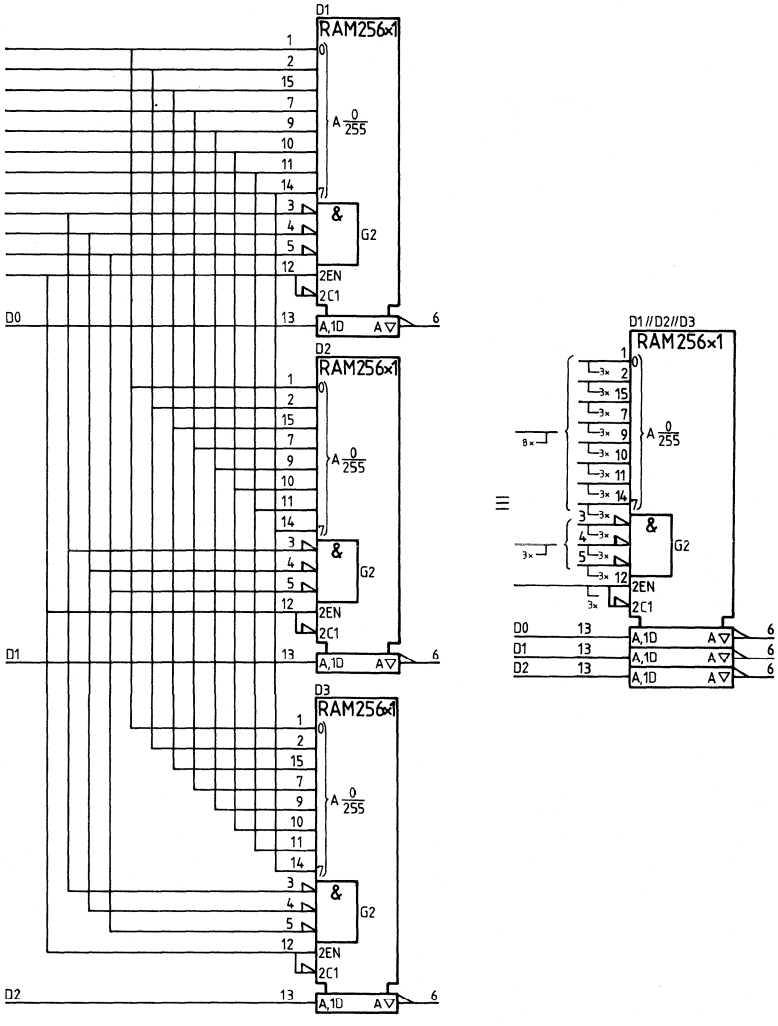


Fig. 46 Example of a multiple symbol showing three TTL "74201" 256x1-bit RAMs connected to lengthen the word.

RULE 8

Every (P)ROM may be regarded as an X/Y-code-converter.

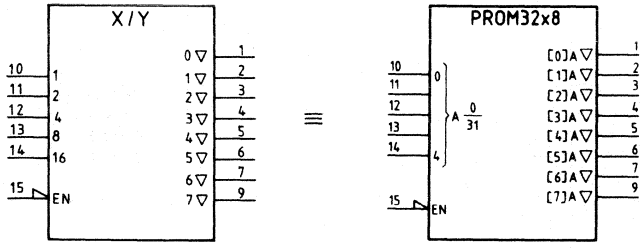
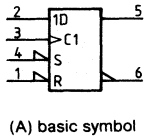


Fig. 47 Example of Rule 8 using Schottky TTL "74S288" PROM.

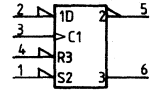
EXAMPLES OF APPLICATION-DEPENDENCY OF SYMBOLS

A symbol depicts the function of an element. In the case of multi-function elements, the functions are depicted separately.

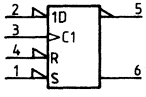
To demonstrate application-dependency of symbols, Fig. 48 shows the basic symbol and eight applications of the "7474" D-element with "S" and "R" inputs.



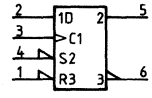
(A) basic symbol



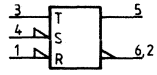
(B) as for (A) but with "R" and "S" dependency



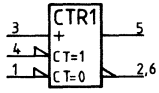
(C) D-input ("L")
(note change of "R" and "S")



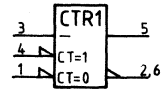
(D) as for (B) but with "S" and "R" dependency



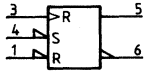
(E) divide-by-2 ("T") element



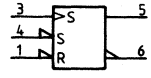
(F) divide-by-2 as a limit case of CTR



(G) as for (F) with down-counter



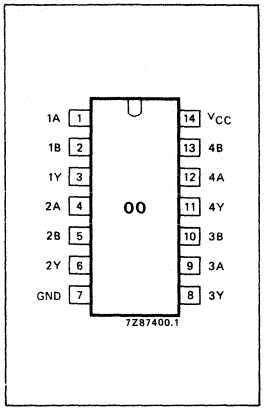
(H) function at pin 2 = "L", or as indicated in a table

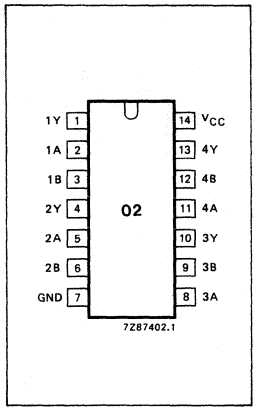


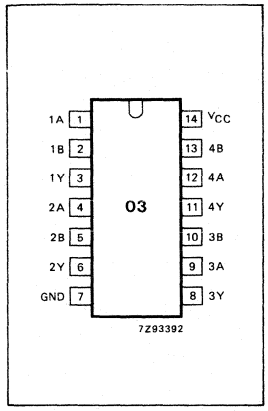
(I) function at pin 2 = "H", or as indicated in a table

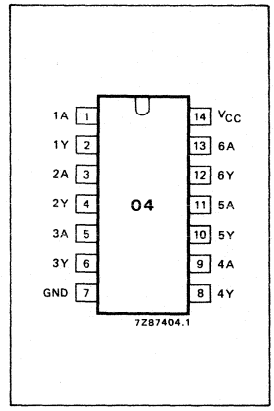
Fig. 48 Example of application-dependent symols for edge-triggered D-element with "R" and "S" inputs.

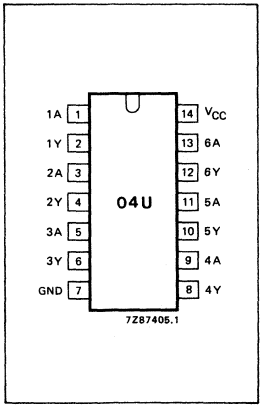
PIN CONFIGURATIONS

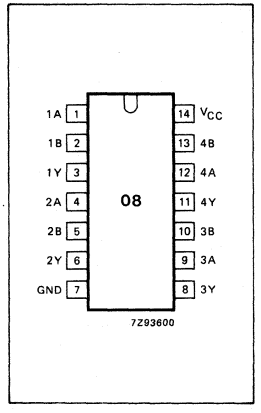

00
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y
7Z87400.1

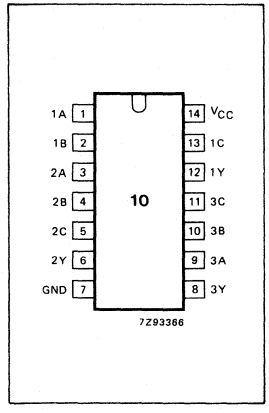

02
1Y 1
1A 2
1B 3
2Y 4
2A 5
2B 6
GND 7
14 VCC
13 4Y
12 4B
11 4A
10 3Y
9 3B
8 3A
7Z87402.1

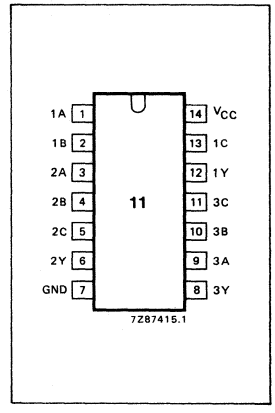

03
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y
7Z93392

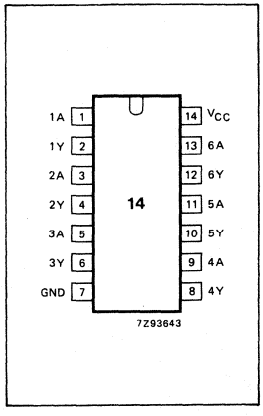

04
1A 1
1Y 2
2A 3
2Y 4
3A 5
3Y 6
GND 7
14 VCC
13 6A
12 6Y
11 5A
10 5Y
9 4A
8 4Y
7Z87404.1

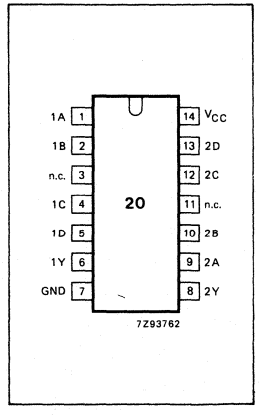

04U
1A 1
1Y 2
2A 3
2Y 4
3A 5
3Y 6
GND 7
14 VCC
13 6A
12 6Y
11 5A
10 5Y
9 4A
8 4Y
7Z87405.1

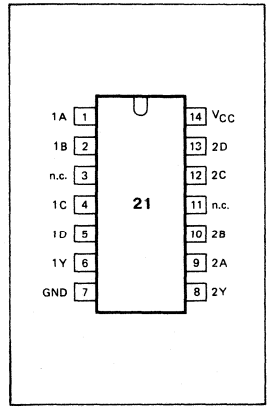

08
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y
7Z93600

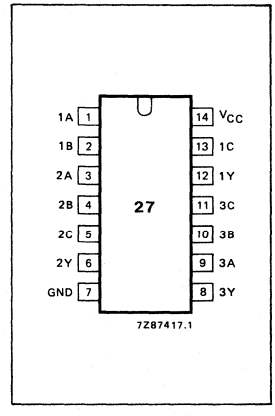

10
1A 1
1B 2
2A 3
2B 4
2C 5
2Y 6
GND 7
14 VCC
13 1C
12 1Y
11 3C
10 3B
9 3A
8 3Y
7Z93366

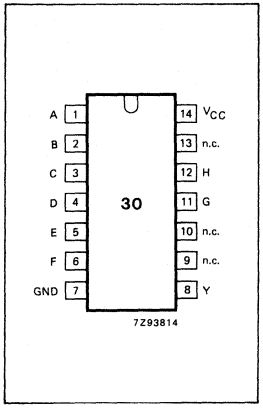

11
1A 1
1B 2
2A 3
2B 4
2C 5
2Y 6
GND 7
14 VCC
13 1C
12 1Y
11 3C
10 3B
9 3A
8 3Y
7Z87415.1

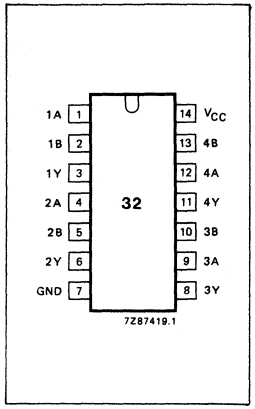

14
1A 1
1Y 2
2A 3
2Y 4
3A 5
3Y 6
GND 7
14 VCC
13 6A
12 6Y
11 5A
10 5Y
9 4A
8 4Y
7Z93643

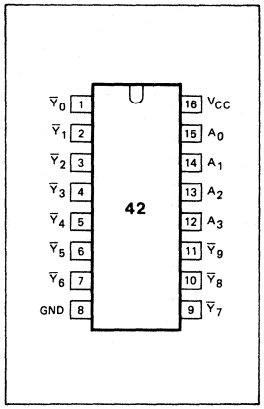

20
1A 1
1B 2
n.c. 3
1C 4
1D 5
1Y 6
GND 7
14 VCC
13 2D
12 2C
11 n.c.
10 2B
9 2A
8 2Y
7Z93762

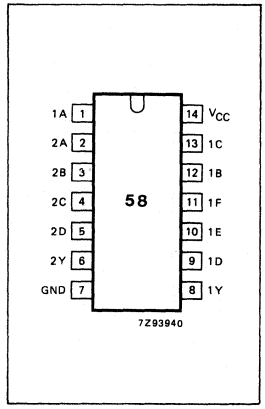

21
1A 1
1B 2
n.c. 3
1C 4
1D 5
1Y 6
GND 7
14 VCC
13 2D
12 2C
11 n.c.
10 2B
9 2A
8 2Y

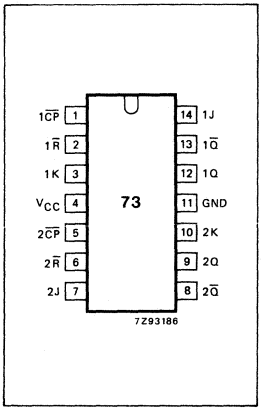

27
1A 1
1B 2
2A 3
2B 4
2C 5
2Y 6
GND 7
14 VCC
13 1C
12 1Y
11 3C
10 3B
9 3A
8 3Y
7Z87417.1

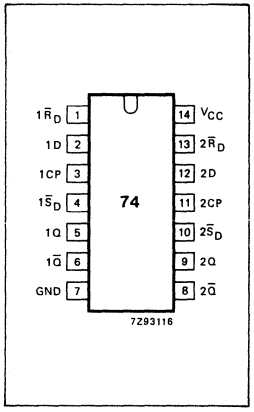

30
A 1
B 2
C 3
D 4
E 5
F 6
GND 7
14 VCC
13 n.c.
12 H
11 G
10 n.c.
9 n.c.
8 Y
7Z93814

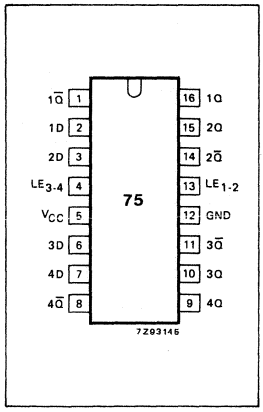

32
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y
7Z87419.1

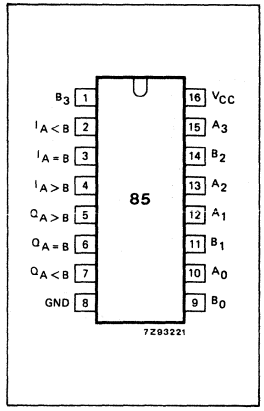

42
$\overline{Y}_0$ 1
$\overline{Y}_1$ 2
$\overline{Y}_2$ 3
$\overline{Y}_3$ 4
$\overline{Y}_4$ 5
$\overline{Y}_5$ 6
$\overline{Y}_6$ 7
GND 8
16 VCC
15 A0
14 A1
13 A2
12 A3
11 $\overline{Y}_9$
10 $\overline{Y}_8$
9 $\overline{Y}_7$

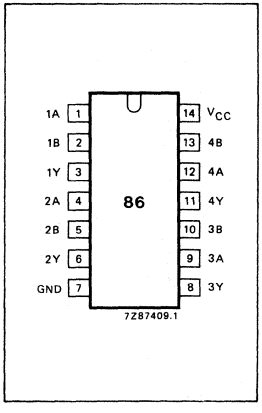

58
1A 1
2A 2
2B 3
2C 4
2D 5
2Y 6
GND 7
14 VCC
13 1C
12 1B
11 1F
10 1E
9 1D
8 1Y
7Z93940

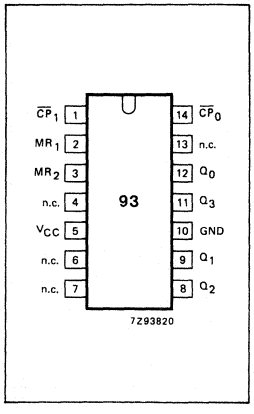

73
1$\overline{CP}$ 1
1$\overline{R}$ 2
1K 3
VCC 4
2$\overline{CP}$ 5
2$\overline{R}$ 6
2J 7
14 1J
13 1$\overline{Q}$
12 1Q
11 GND
10 2K
9 2Q
8 2$\overline{Q}$
7Z93186

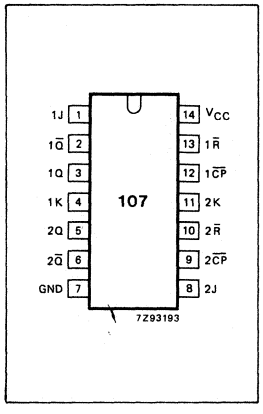

74
1$\overline{R}_D$ 1
1D 2
1CP 3
1$\overline{S}_D$ 4
1Q 5
1$\overline{Q}$ 6
GND 7
14 VCC
13 2$\overline{R}_D$
12 2D
11 2CP
10 2$\overline{S}_D$
9 2Q
8 2$\overline{Q}$
7Z93116

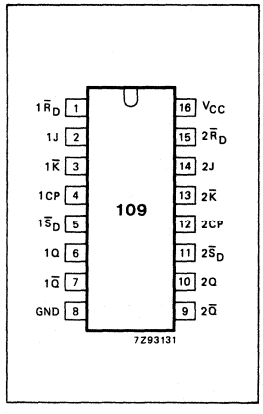

75
1$\overline{Q}$ 1
1D 2
2D 3
LE3-4 4
VCC 5
3D 6
4D 7
4$\overline{Q}$ 8
16 1Q
15 2Q
14 2$\overline{Q}$
13 LE1-2
12 GND
11 3$\overline{Q}$
10 3Q
9 4Q
7Z93146

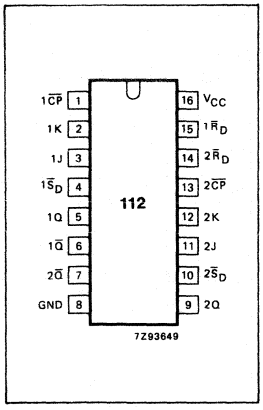

85
B3 1
IA<B 2
IA=B 3
IA>B 4
QA>B 5
QA=B 6
QA<B 7
GND 8
16 VCC
15 A3
14 B2
13 A2
12 A1
11 B1
10 A0
9 B0
7Z93221

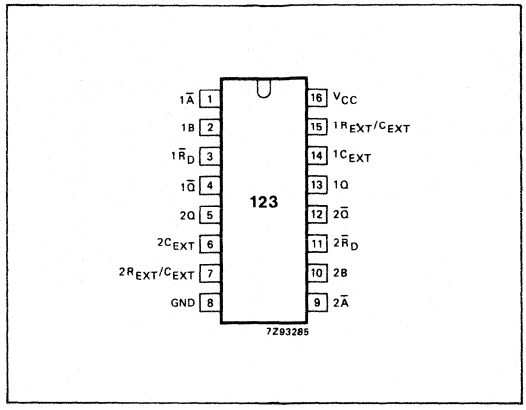

86
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y
7Z87409.1

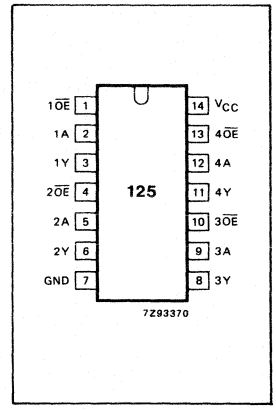

93
$\overline{CP}_1$ 1
MR1 2
MR2 3
n.c. 4
VCC 5
n.c. 6
n.c. 7
14 $\overline{CP}_0$
13 n.c.
12 Q0
11 Q3
10 GND
9 Q1
8 Q2
7Z93820

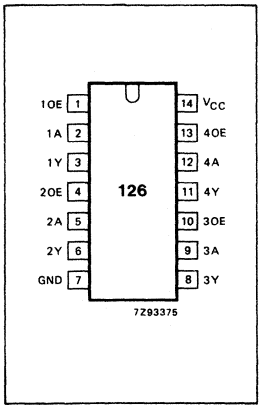

107
1J 1
1$\overline{Q}$ 2
1Q 3
1K 4
2Q 5
2$\overline{Q}$ 6
GND 7
14 VCC
13 1$\overline{R}$
12 1$\overline{CP}$
11 2K
10 2$\overline{R}$
9 2$\overline{CP}$
8 2J
7Z93193

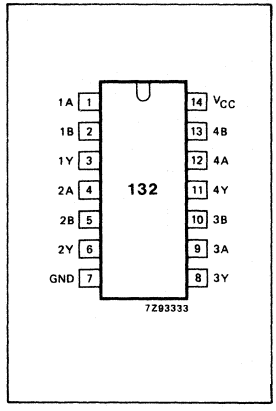

109
1$\overline{R}_D$ 1
1J 2
1$\overline{K}$ 3
1CP 4
1$\overline{S}_D$ 5
1Q 6
1$\overline{Q}$ 7
GND 8
16 VCC
15 2$\overline{R}_D$
14 2J
13 2$\overline{K}$
12 2CP
11 2$\overline{S}_D$
10 2Q
9 2$\overline{Q}$
7Z93131

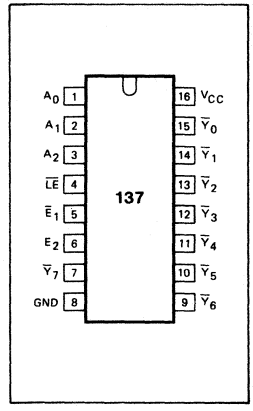

112
1$\overline{CP}$ 1
1K 2
1J 3
1$\overline{S}_D$ 4
1Q 5
1$\overline{Q}$ 6
2$\overline{Q}$ 7
GND 8
16 V_{CC}
15 1$\overline{R}_D$
14 2$\overline{R}_D$
13 2$\overline{CP}$
12 2K
11 2J
10 2$\overline{S}_D$
9 2Q
7Z93649

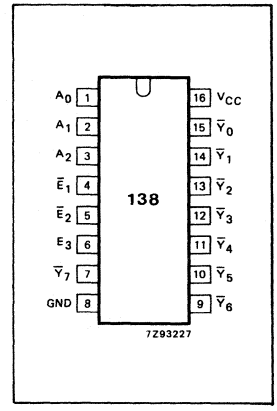

123
1$\overline{A}$ 1
1B 2
1$\overline{R}_D$ 3
1$\overline{Q}$ 4
2Q 5
$2C_{EXT}$ 6
$2R_{EXT}/C_{EXT}$ 7
GND 8
16 V_{CC}
15 $1R_{EXT}/C_{EXT}$
14 $1C_{EXT}$
13 1Q
12 2$\overline{Q}$
11 2$\overline{R}_D$
10 2B
9 2$\overline{A}$
7Z93285

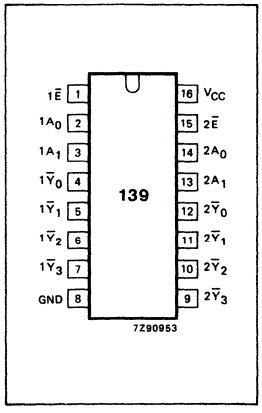

125
1$\overline{OE}$ 1
1A 2
1Y 3
2$\overline{OE}$ 4
2A 5
2Y 6
GND 7
14 V_{CC}
13 4$\overline{OE}$
12 4A
11 4Y
10 3$\overline{OE}$
9 3A
8 3Y
7Z93370

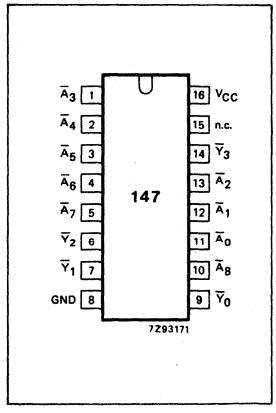

126
1OE 1
1A 2
1Y 3
2OE 4
2A 5
2Y 6
GND 7
14 V_{CC}
13 4OE
12 4A
11 4Y
10 3OE
9 3A
8 3Y
7Z93375

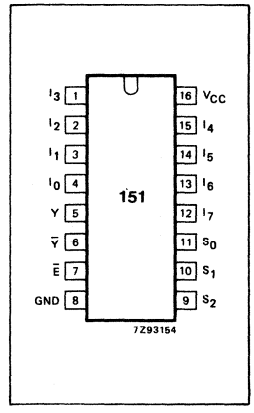

132
1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 V_{CC}
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y
7Z93333

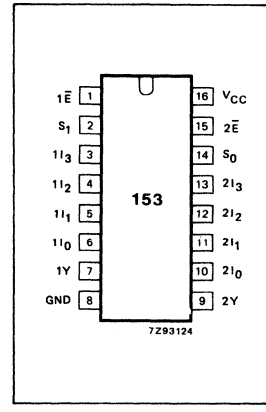

137
A_0 1
A_1 2
A_2 3
$\overline{LE}$ 4
$\overline{E}_1$ 5
E_2 6
$\overline{Y}_7$ 7
GND 8
16 V_{CC}
15 $\overline{Y}_0$
14 $\overline{Y}_1$
13 $\overline{Y}_2$
12 $\overline{Y}_3$
11 $\overline{Y}_4$
10 $\overline{Y}_5$
9 $\overline{Y}_6$

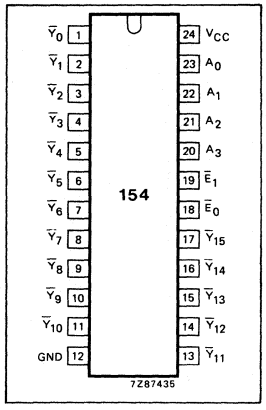

138
A_0 1
A_1 2
A_2 3
$\overline{E}_1$ 4
$\overline{E}_2$ 5
E_3 6
$\overline{Y}_7$ 7
GND 8
16 V_{CC}
15 $\overline{Y}_0$
14 $\overline{Y}_1$
13 $\overline{Y}_2$
12 $\overline{Y}_3$
11 $\overline{Y}_4$
10 $\overline{Y}_5$
9 $\overline{Y}_6$
7Z93227

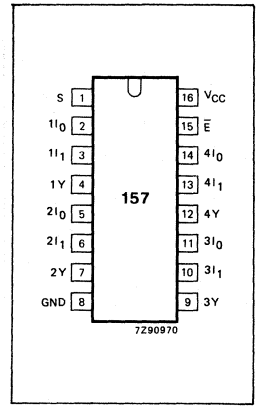

139
1$\overline{E}$ 1
$1A_0$ 2
$1A_1$ 3
$1\overline{Y}_0$ 4
$1\overline{Y}_1$ 5
$1\overline{Y}_2$ 6
$1\overline{Y}_3$ 7
GND 8
16 V_{CC}
15 2$\overline{E}$
14 $2A_0$
13 $2A_1$
12 $2\overline{Y}_0$
11 $2\overline{Y}_1$
10 $2\overline{Y}_2$
9 $2\overline{Y}_3$
7Z90953

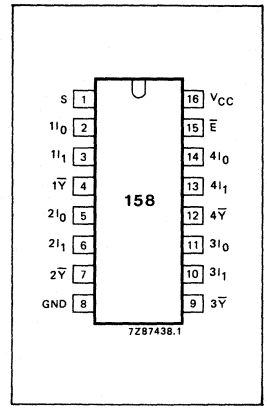

147
$\overline{A}_3$ 1
$\overline{A}_4$ 2
$\overline{A}_5$ 3
$\overline{A}_6$ 4
$\overline{A}_7$ 5
$\overline{Y}_2$ 6
$\overline{Y}_1$ 7
GND 8
16 V_{CC}
15 n.c.
14 $\overline{Y}_3$
13 $\overline{A}_2$
12 $\overline{A}_1$
11 $\overline{A}_0$
10 $\overline{A}_8$
9 $\overline{Y}_0$
7Z93171

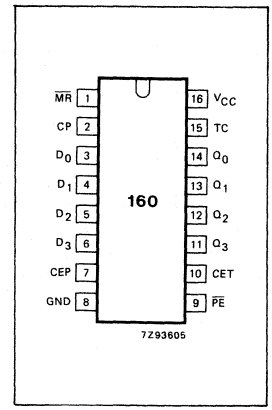

151
I_3 1
I_2 2
I_1 3
I_0 4
Y 5
$\overline{Y}$ 6
$\overline{E}$ 7
GND 8
16 V_{CC}
15 I_4
14 I_5
13 I_6
12 I_7
11 S_0
10 S_1
9 S_2
7Z93154

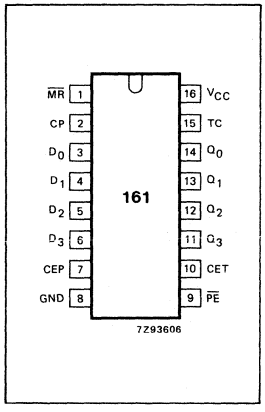

153
1$\overline{E}$ 1
S_1 2
$1I_3$ 3
$1I_2$ 4
$1I_1$ 5
$1I_0$ 6
1Y 7
GND 8
16 V_{CC}
15 2$\overline{E}$
14 S_0
13 $2I_3$
12 $2I_2$
11 $2I_1$
10 $2I_0$
9 2Y
7Z93124

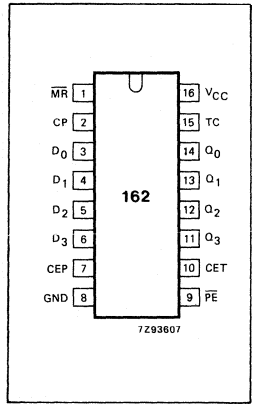

154
$\overline{Y}_0$ 1
$\overline{Y}_1$ 2
$\overline{Y}_2$ 3
$\overline{Y}_3$ 4
$\overline{Y}_4$ 5
$\overline{Y}_5$ 6
$\overline{Y}_6$ 7
$\overline{Y}_7$ 8
$\overline{Y}_8$ 9
$\overline{Y}_9$ 10
$\overline{Y}_{10}$ 11
GND 12
24 V_{CC}
23 A_0
22 A_1
21 A_2
20 A_3
19 $\overline{E}_1$
18 $\overline{E}_0$
17 $\overline{Y}_{15}$
16 $\overline{Y}_{14}$
15 $\overline{Y}_{13}$
14 $\overline{Y}_{12}$
13 $\overline{Y}_{11}$
7Z87435

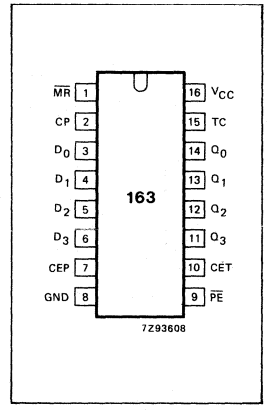

157
S 1
$1I_0$ 2
$1I_1$ 3
1Y 4
$2I_0$ 5
$2I_1$ 6
2Y 7
GND 8
16 V_{CC}
15 $\overline{E}$
14 $4I_0$
13 $4I_1$
12 4Y
11 $3I_0$
10 $3I_1$
9 3Y
7Z90970

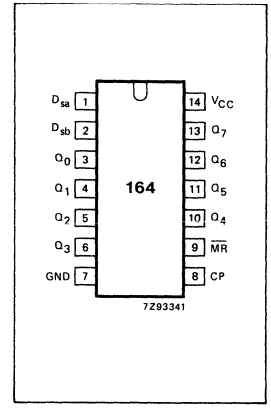

158
S 1
$1I_0$ 2
$1I_1$ 3
$1\overline{Y}$ 4
$2I_0$ 5
$2I_1$ 6
$2\overline{Y}$ 7
GND 8
16 V_{CC}
15 $\overline{E}$
14 $4I_0$
13 $4I_1$
12 $4\overline{Y}$
11 $3I_0$
10 $3I_1$
9 $3\overline{Y}$
7Z87438.1

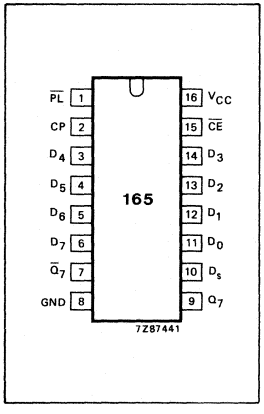

160
$\overline{MR}$ 1
CP 2
D_0 3
D_1 4
D_2 5
D_3 6
CEP 7
GND 8
16 V_{CC}
15 TC
14 Q_0
13 Q_1
12 Q_2
11 Q_3
10 CET
9 $\overline{PE}$
7Z93605

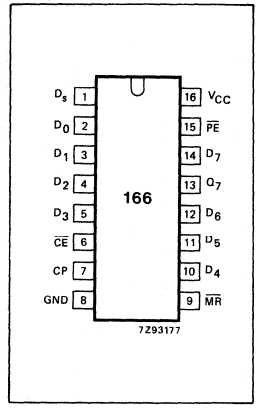

161
$\overline{MR}$ 1
CP 2
D_0 3
D_1 4
D_2 5
D_3 6
CEP 7
GND 8
16 V_{CC}
15 TC
14 Q_0
13 Q_1
12 Q_2
11 Q_3
10 CET
9 $\overline{PE}$
7Z93606

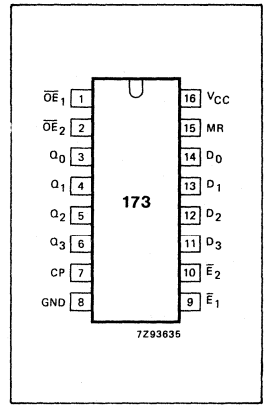

162
$\overline{MR}$ 1
CP 2
D_0 3
D_1 4
D_2 5
D_3 6
CEP 7
GND 8
16 V_{CC}
15 TC
14 Q_0
13 Q_1
12 Q_2
11 Q_3
10 CET
9 $\overline{PE}$
7Z93607

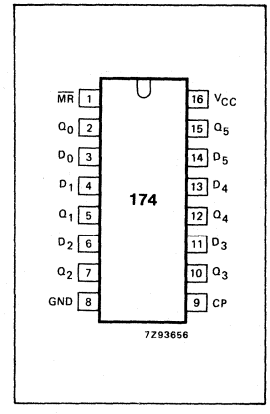

163
$\overline{MR}$ 1
CP 2
D_0 3
D_1 4
D_2 5
D_3 6
CEP 7
GND 8
16 V_{CC}
15 TC
14 Q_0
13 Q_1
12 Q_2
11 Q_3
10 CET
9 $\overline{PE}$
7Z93608

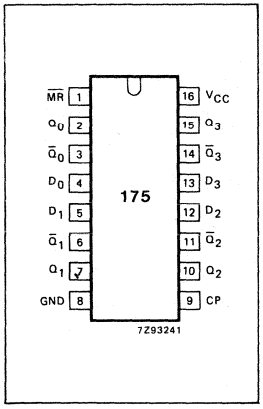

164
D_{sa} 1
D_{sb} 2
Q_0 3
Q_1 4
Q_2 5
Q_3 6
GND 7
14 V_{CC}
13 Q_7
12 Q_6
11 Q_5
10 Q_4
9 $\overline{MR}$
8 CP
7Z93341

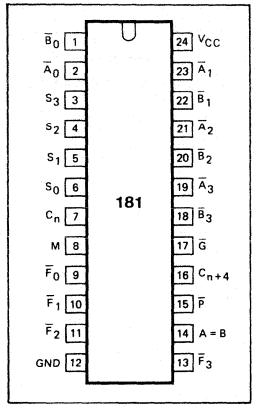

165
$\overline{PL}$ 1
CP 2
D_4 3
D_5 4
D_6 5
D_7 6
$\overline{Q}_7$ 7
GND 8
16 V_{CC}
15 $\overline{CE}$
14 D_3
13 D_2
12 D_1
11 D_0
10 D_s
9 Q_7
7Z87441

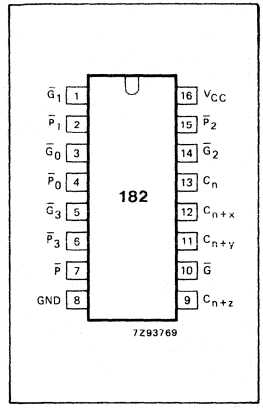

166
D_s 1
D_0 2
D_1 3
D_2 4
D_3 5
$\overline{CE}$ 6
CP 7
GND 8
16 V_{CC}
15 $\overline{PE}$
14 D_7
13 Q_7
12 D_6
11 D_5
10 D_4
9 $\overline{MR}$
7Z93177

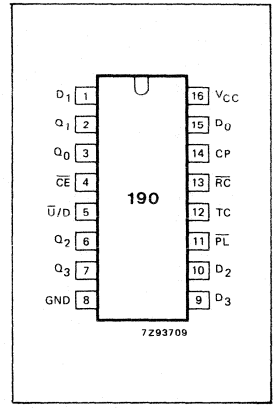

173
$\overline{OE}_1$ 1
$\overline{OE}_2$ 2
Q_0 3
Q_1 4
Q_2 5
Q_3 6
CP 7
GND 8
16 V_{CC}
15 MR
14 D_0
13 D_1
12 D_2
11 D_3
10 $\overline{E}_2$
9 $\overline{E}_1$
7Z93635

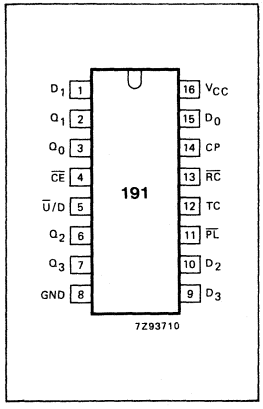

174
$\overline{MR}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
D_2 6
Q_2 7
GND 8
16 V_{CC}
15 Q_5
14 D_5
13 D_4
12 Q_4
11 D_3
10 Q_3
9 CP
7Z93656

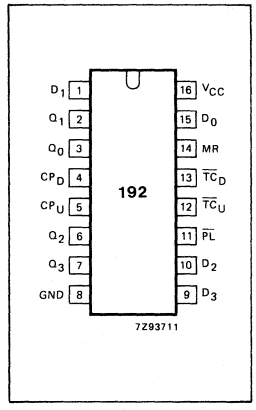

175
MR 1
Q0 2
Q̄0 3
D0 4
D1 5
Q̄1 6
Q1 7
GND 8
16 VCC
15 Q3
14 Q̄3
13 D3
12 D2
11 Q̄2
10 Q2
9 CP
7Z93241

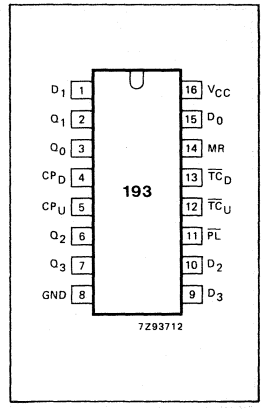

181
B̄0 1
Ā0 2
S3 3
S2 4
S1 5
S0 6
Cn 7
M 8
F̄0 9
F̄1 10
F̄2 11
GND 12
24 VCC
23 Ā1
22 B̄1
21 Ā2
20 B̄2
19 Ā3
18 B̄3
17 Ḡ
16 Cn+4
15 P̄
14 A = B
13 F̄3

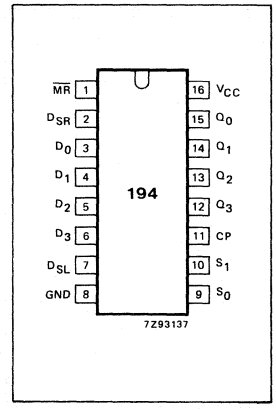

182
Ḡ1 1
P̄1 2
Ḡ0 3
P̄0 4
Ḡ3 5
P̄3 6
P̄ 7
GND 8
16 VCC
15 P̄2
14 Ḡ2
13 Cn
12 Cn+x
11 Cn+y
10 Ḡ
9 Cn+z
7Z93769

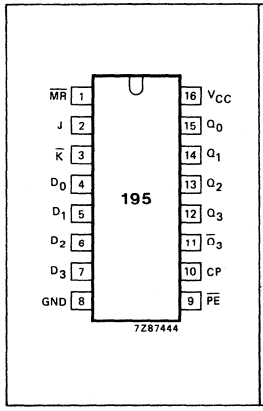

190
D1 1
Q1 2
Q0 3
CE 4
U/D 5
Q2 6
Q3 7
GND 8
16 VCC
15 D0
14 CP
13 RC
12 TC
11 PL
10 D2
9 D3
7Z93709

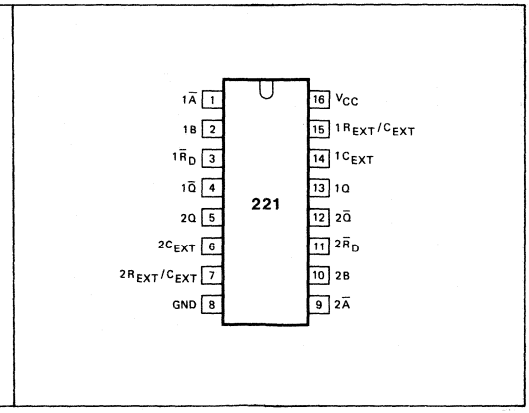

191
D1 1
Q1 2
Q0 3
CE 4
U/D 5
Q2 6
Q3 7
GND 8
16 VCC
15 D0
14 CP
13 RC
12 TC
11 PL
10 D2
9 D3
7Z93710

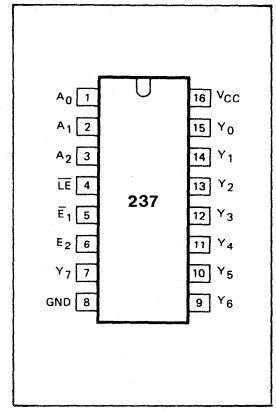

192
D1 1
Q1 2
Q0 3
CPD 4
CPU 5
Q2 6
Q3 7
GND 8
16 VCC
15 D0
14 MR
13 TCD
12 TCU
11 PL
10 D2
9 D3
7Z93711

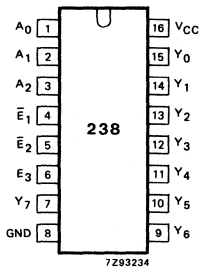

193
D1 1
Q1 2
Q0 3
CPD 4
CPU 5
Q2 6
Q3 7
GND 8
16 VCC
15 D0
14 MR
13 TCD
12 TCU
11 PL
10 D2
9 D3
7Z93712

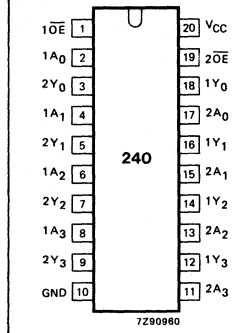

194
MR 1
DSR 2
D0 3
D1 4
D2 5
D3 6
DSL 7
GND 8
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 CP
10 S1
9 S0
7Z93137

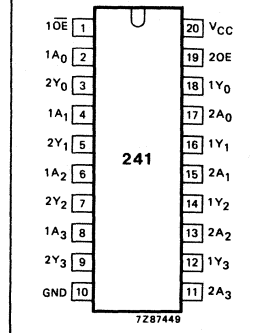

195
MR 1
J 2
K̄ 3
D0 4
D1 5
D2 6
D3 7
GND 8
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 Q̄3
10 CP
9 PE
7Z87444

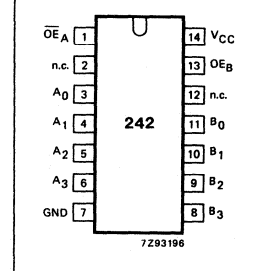

221
1Ā 1
1B 2
1R̄D 3
1Q̄ 4
2Q 5
2CEXT 6
2REXT/CEXT 7
GND 8
16 VCC
15 1REXT/CEXT
14 1CEXT
13 1Q
12 2Q̄
11 2R̄D
10 2B
9 2Ā

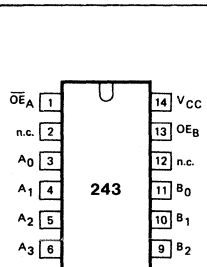

237
A0 1
A1 2
A2 3
LE 4
Ē1 5
E2 6
Y7 7
GND 8
16 VCC
15 Y0
14 Y1
13 Y2
12 Y3
11 Y4
10 Y5
9 Y6

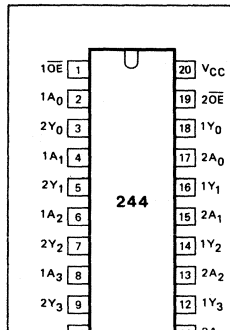

238
A0 1
A1 2
A2 3
E1 4
E2 5
E3 6
Y7 7
GND 8
16 VCC
15 Y0
14 Y1
13 Y2
12 Y3
11 Y4
10 Y5
9 Y6
7Z93234

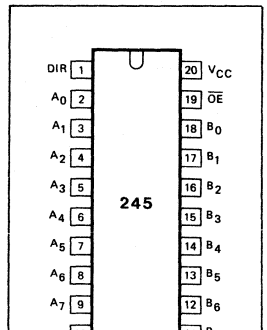

240
1OE 1
1A0 2
2Y0 3
1A1 4
2Y1 5
1A2 6
2Y2 7
1A3 8
2Y3 9
GND 10
20 VCC
19 2OE
18 1Y0
17 2A0
16 1Y1
15 2A1
14 1Y2
13 2A2
12 1Y3
11 2A3
7Z90960

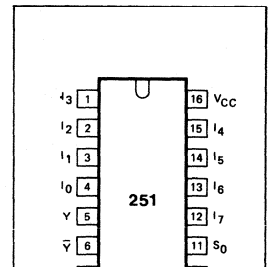

241
1OE 1
1A0 2
2Y0 3
1A1 4
2Y1 5
1A2 6
2Y2 7
1A3 8
2Y3 9
GND 10
20 VCC
19 2OE
18 1Y0
17 2A0
16 1Y1
15 2A1
14 1Y2
13 2A2
12 1Y3
11 2A3
7Z87449

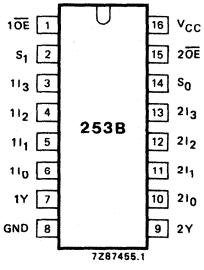

242
OEA 1
n.c. 2
A0 3
A1 4
A2 5
A3 6
GND 7
14 VCC
13 OEB
12 n.c.
11 B0
10 B1
9 B2
8 B3
7Z93196

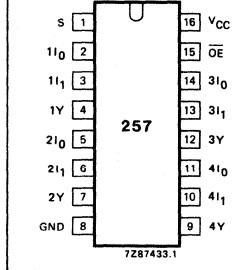

243
OEA 1
n.c. 2
A0 3
A1 4
A2 5
A3 6
GND 7
14 VCC
13 OEB
12 n.c.
11 B0
10 B1
9 B2
8 B3
7Z93203

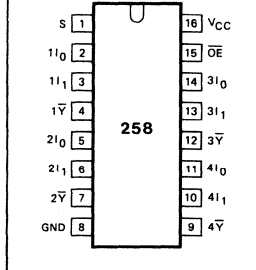

244
1OE 1
1A0 2
2Y0 3
1A1 4
2Y1 5
1A2 6
2Y2 7
1A3 8
2Y3 9
GND 10
20 VCC
19 2OE
18 1Y0
17 2A0
16 1Y1
15 2A1
14 1Y2
13 2A2
12 1Y3
11 2A3
7Z87451

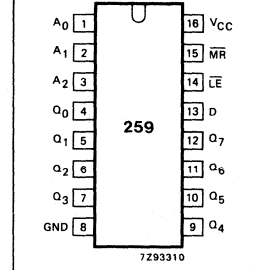

245
DIR 1
A0 2
A1 3
A2 4
A3 5
A4 6
A5 7
A6 8
A7 9
GND 10
20 VCC
19 OE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
7Z87453

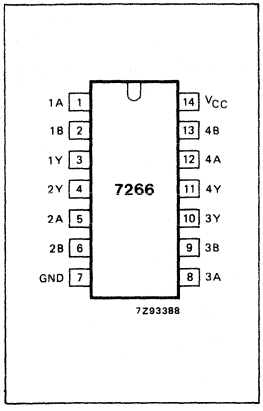

251
I3 1
I2 2
I1 3
I0 4
Y 5
Y 6
OE 7
GND 8
16 VCC
15 I4
14 I5
13 I6
12 I7
11 S0
10 S1
9 S2
7Z93100

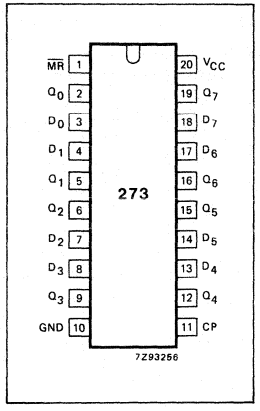

253B
1OE 1
S1 2
1I3 3
1I2 4
1I1 5
1I0 6
1Y 7
GND 8
16 VCC
15 2OE
14 S0
13 2I3
12 2I2
11 2I1
10 2I0
9 2Y
7Z87455.1

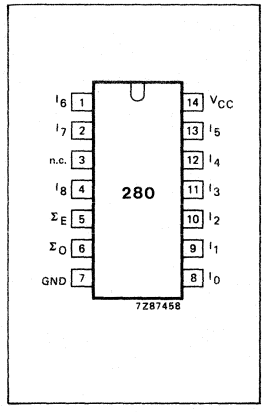

257
S 1
1I0 2
1I1 3
1Y 4
2I0 5
2I1 6
2Y 7
GND 8
16 VCC
15 OE
14 3I0
13 3I1
12 3Y
11 4I0
10 4I1
9 4Y
7Z87433.1

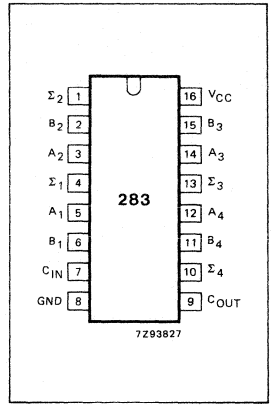

258
S 1
1I0 2
1I1 3
1Y 4
2I0 5
2I1 6
2Y 7
GND 8
16 VCC
15 OE
14 3I0
13 3I1
12 3Y
11 4I0
10 4I1
9 4Y

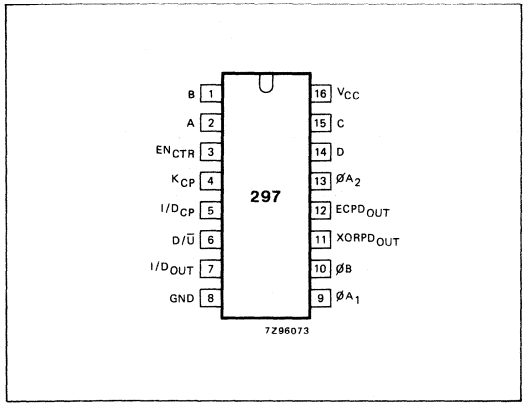

259
A0 1
A1 2
A2 3
Q0 4
Q1 5
Q2 6
Q3 7
GND 8
16 VCC
15 MR
14 LE
13 D
12 Q7
11 Q6
10 Q5
9 Q4
7Z93310

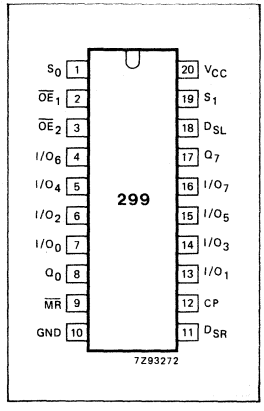

7266
1A 1
1B 2
1Y 3
2Y 4
2A 5
2B 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3Y
9 3B
8 3A
7Z93388

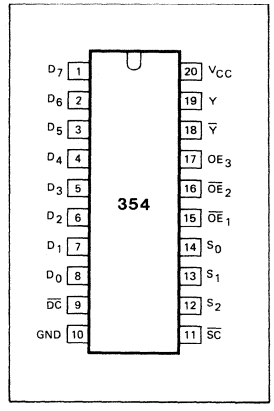

273
MR 1
Q0 2
D0 3
D1 4
Q1 5
Q2 6
D2 7
D3 8
Q3 9
GND 10
20 VCC
19 Q7
18 D7
17 D6
16 Q6
15 Q5
14 D5
13 D4
12 Q4
11 CP
7Z93256

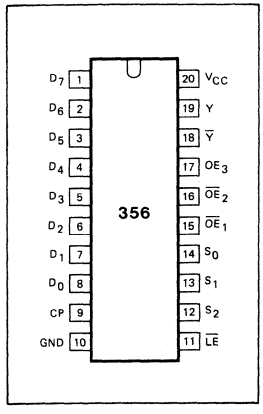

280
I6 1
I7 2
n.c. 3
I8 4
ΣE 5
ΣO 6
GND 7
14 VCC
13 I5
12 I4
11 I3
10 I2
9 I1
8 I0
7Z87458

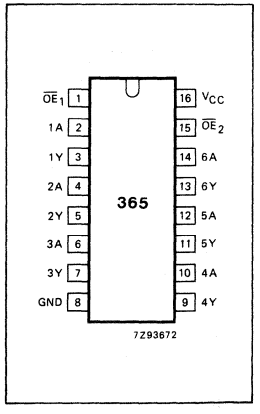

283
Σ2 1
B2 2
A2 3
Σ1 4
A1 5
B1 6
CIN 7
GND 8
16 VCC
15 B3
14 A3
13 Σ3
12 A4
11 B4
10 Σ4
9 COUT
7Z93827

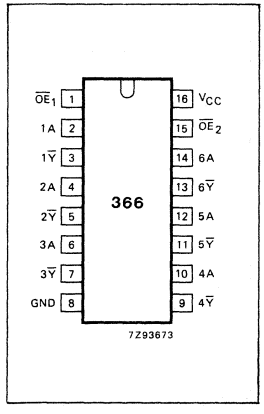

297
B 1
A 2
ENCTR 3
KCP 4
I/DCP 5
D/U 6
I/DOUT 7
GND 8
16 VCC
15 C
14 D
13 ØA2
12 ECPDOUT
11 XORPDOUT
10 ØB
9 ØA1
7Z96073

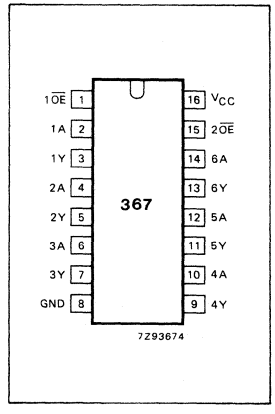

299
S0 1
OE1 2
OE2 3
I/O6 4
I/O4 5
I/O2 6
I/O0 7
Q0 8
MR 9
GND 10
20 VCC
19 S1
18 DSL
17 Q7
16 I/O7
15 I/O5
14 I/O3
13 I/O1
12 CP
11 DSR
7Z93272

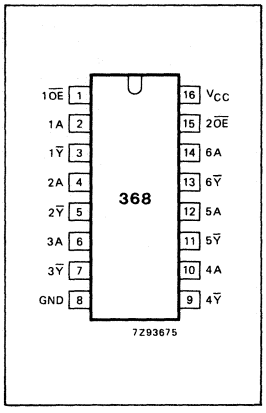

354
D7 1
D6 2
D5 3
D4 4
D3 5
D2 6
D1 7
D0 8
DC 9
GND 10
20 VCC
19 Y
18 Y
17 OE3
16 OE2
15 OE1
14 S0
13 S1
12 S2
11 SC

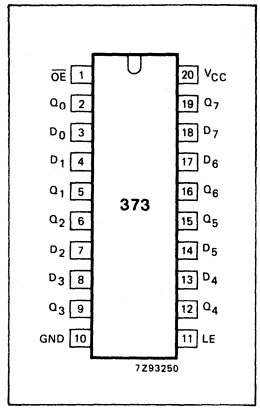

356
D7 1
D6 2
D5 3
D4 4
D3 5
D2 6
D1 7
D0 8
CP 9
GND 10
20 VCC
19 Y
18 Y
17 OE3
16 OE2
15 OE1
14 S0
13 S1
12 S2
11 LE

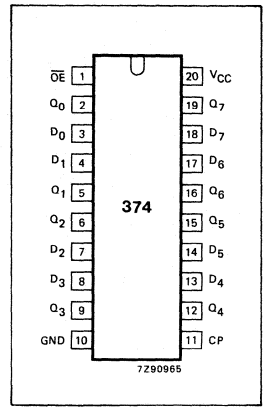

365
OE1 1
1A 2
1Y 3
2A 4
2Y 5
3A 6
3Y 7
GND 8
16 VCC
15 OE2
14 6A
13 6Y
12 5A
11 5Y
10 4A
9 4Y
7Z93672

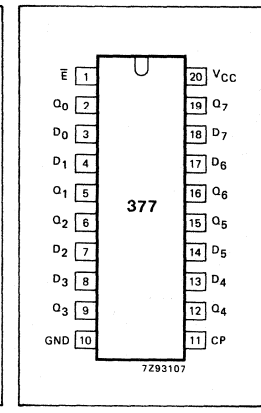

366
OE1 1
1A 2
1Y 3
2A 4
2Y 5
3A 6
3Y 7
GND 8
16 VCC
15 OE2
14 6A
13 6Y
12 5A
11 5Y
10 4A
9 4Y
7Z93673

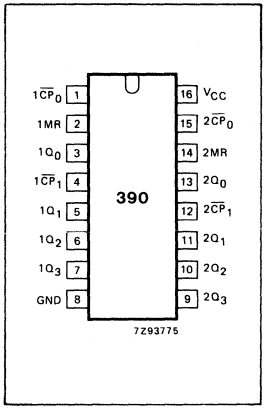

367
1OE 1
1A 2
1Y 3
2A 4
2Y 5
3A 6
3Y 7
GND 8
16 VCC
15 2OE
14 6A
13 6Y
12 5A
11 5Y
10 4A
9 4Y
7Z93674

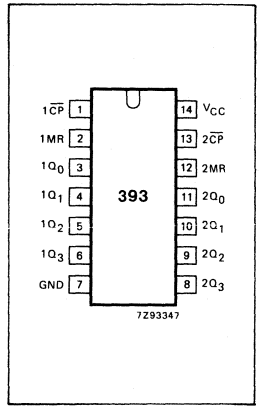

368
1$\overline{OE}$ 1
1A 2
1$\overline{Y}$ 3
2A 4
2$\overline{Y}$ 5
3A 6
3$\overline{Y}$ 7
GND 8
16 V_{CC}
15 2$\overline{OE}$
14 6A
13 6$\overline{Y}$
12 5A
11 5$\overline{Y}$
10 4A
9 4$\overline{Y}$
7Z93675

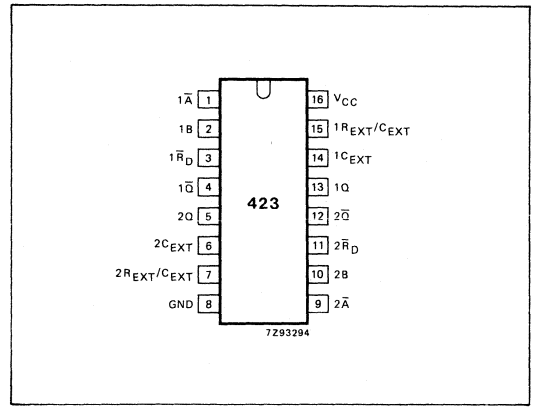

373
$\overline{OE}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 LE
7Z93250

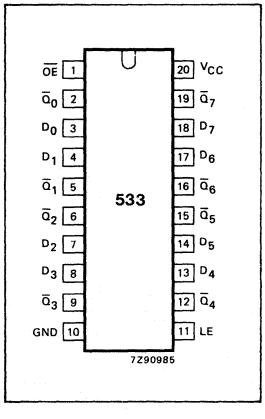

374
$\overline{OE}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 CP
7Z90965

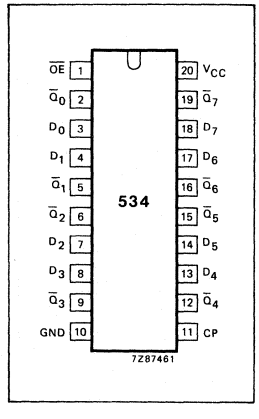

377
$\overline{E}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 CP
7Z93107

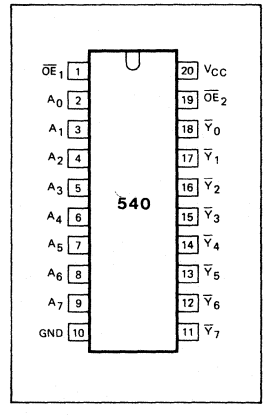

390
1$\overline{CP}_0$ 1
1MR 2
1Q_0 3
1$\overline{CP}_1$ 4
1Q_1 5
1Q_2 6
1Q_3 7
GND 8
16 V_{CC}
15 2$\overline{CP}_0$
14 2MR
13 2Q_0
12 2$\overline{CP}_1$
11 2Q_1
10 2Q_2
9 2Q_3
7Z93775

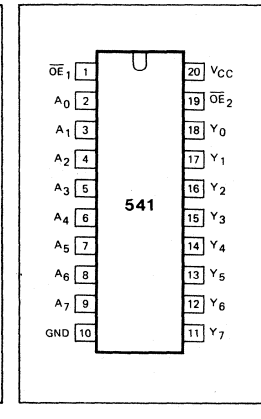

393
1$\overline{CP}$ 1
1MR 2
1Q_0 3
1Q_1 4
1Q_2 5
1Q_3 6
GND 7
14 V_{CC}
13 2$\overline{CP}$
12 2MR
11 2Q_0
10 2Q_1
9 2Q_2
8 2Q_3
7Z93347

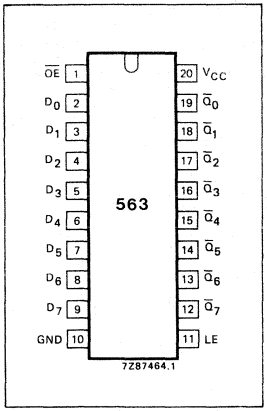

423
1$\overline{A}$ 1
1B 2
1$\overline{R}_D$ 3
1$\overline{Q}$ 4
2Q 5
$2C_{EXT}$ 6
$2R_{EXT}/C_{EXT}$ 7
GND 8
16 V_{CC}
15 $1R_{EXT}/C_{EXT}$
14 $1C_{EXT}$
13 1Q
12 2$\overline{Q}$
11 2$\overline{R}_D$
10 2B
9 2$\overline{A}$
7Z93294

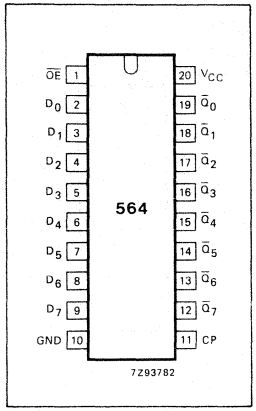

533
$\overline{OE}$ 1
$\overline{Q}_0$ 2
D_0 3
D_1 4
$\overline{Q}_1$ 5
$\overline{Q}_2$ 6
D_2 7
D_3 8
$\overline{Q}_3$ 9
GND 10
20 V_{CC}
19 $\overline{Q}_7$
18 D_7
17 D_6
16 $\overline{Q}_6$
15 $\overline{Q}_5$
14 D_5
13 D_4
12 $\overline{Q}_4$
11 LE
7Z90985

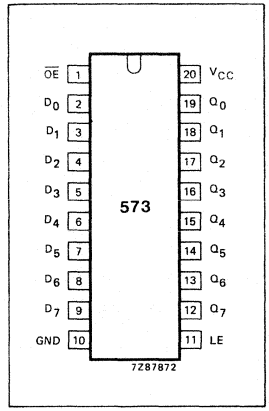

534
$\overline{OE}$ 1
$\overline{Q}_0$ 2
D_0 3
D_1 4
$\overline{Q}_1$ 5
$\overline{Q}_2$ 6
D_2 7
D_3 8
$\overline{Q}_3$ 9
GND 10
20 V_{CC}
19 $\overline{Q}_7$
18 D_7
17 D_6
16 $\overline{Q}_6$
15 $\overline{Q}_5$
14 D_5
13 D_4
12 $\overline{Q}_4$
11 CP
7Z87461

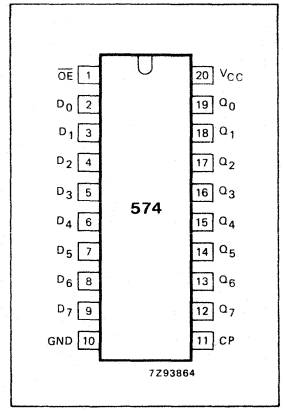

540
$\overline{OE}_1$ 1
A_0 2
A_1 3
A_2 4
A_3 5
A_4 6
A_5 7
A_6 8
A_7 9
GND 10
20 V_{CC}
19 $\overline{OE}_2$
18 $\overline{Y}_0$
17 $\overline{Y}_1$
16 $\overline{Y}_2$
15 $\overline{Y}_3$
14 $\overline{Y}_4$
13 $\overline{Y}_5$
12 $\overline{Y}_6$
11 $\overline{Y}_7$

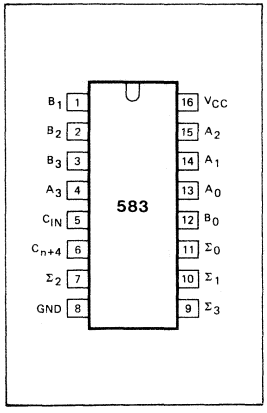

541
$\overline{OE}_1$ 1
A_0 2
A_1 3
A_2 4
A_3 5
A_4 6
A_5 7
A_6 8
A_7 9
GND 10
20 V_{CC}
19 $\overline{OE}_2$
18 Y_0
17 Y_1
16 Y_2
15 Y_3
14 Y_4
13 Y_5
12 Y_6
11 Y_7

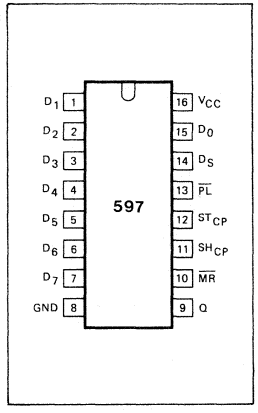

563
1 OE
2 D0
3 D1
4 D2
5 D3
6 D4
7 D5
8 D6
9 D7
10 GND
20 VCC
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 LE
7Z87464.1

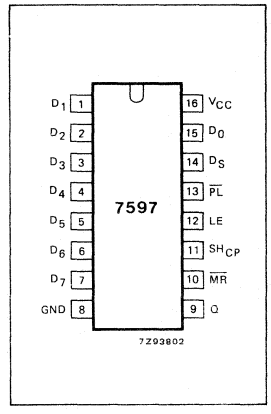

564
1 OE
2 D0
3 D1
4 D2
5 D3
6 D4
7 D5
8 D6
9 D7
10 GND
20 VCC
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 CP
7Z93782

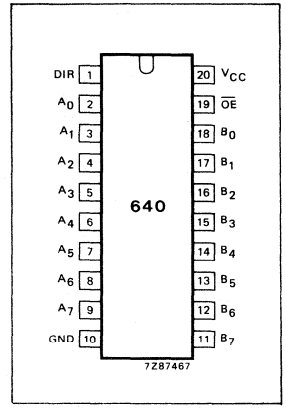

573
1 OE
2 D0
3 D1
4 D2
5 D3
6 D4
7 D5
8 D6
9 D7
10 GND
20 VCC
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 LE
7Z87872

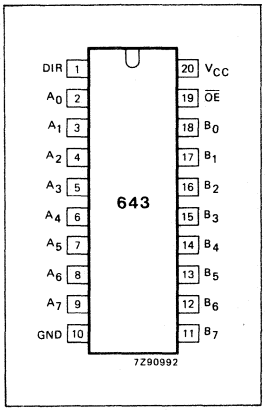

574
1 OE
2 D0
3 D1
4 D2
5 D3
6 D4
7 D5
8 D6
9 D7
10 GND
20 VCC
19 Q0
18 Q1
17 Q2
16 Q3
15 Q4
14 Q5
13 Q6
12 Q7
11 CP
7Z93864

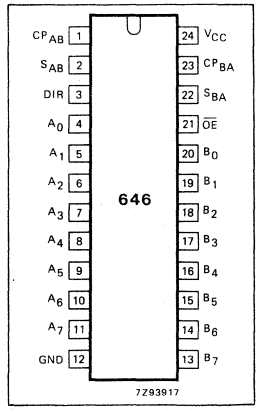

583
1 B1
2 B2
3 B3
4 A3
5 CIN
6 Cn+4
7 Σ2
8 GND
16 VCC
15 A2
14 A1
13 A0
12 B0
11 Σ0
10 Σ1
9 Σ3

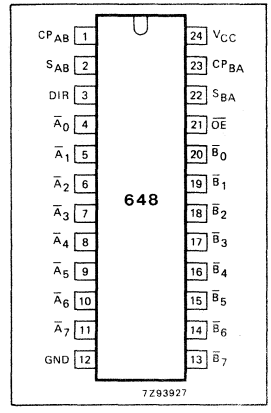

597
1 D1
2 D2
3 D3
4 D4
5 D5
6 D6
7 D7
8 GND
16 VCC
15 D0
14 DS
13 PL
12 STCP
11 SHCP
10 MR
9 Q

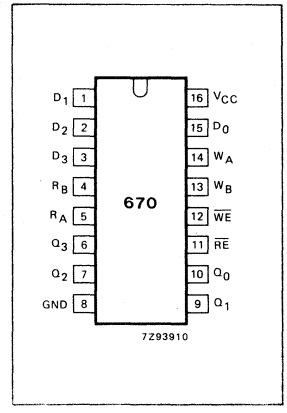

7597
1 D1
2 D2
3 D3
4 D4
5 D5
6 D6
7 D7
8 GND
16 VCC
15 D0
14 DS
13 PL
12 LE
11 SHCP
10 MR
9 Q
7Z93802

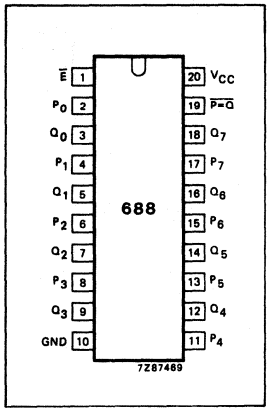

640
1 DIR
2 A0
3 A1
4 A2
5 A3
6 A4
7 A5
8 A6
9 A7
10 GND
20 VCC
19 OE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
7Z87467

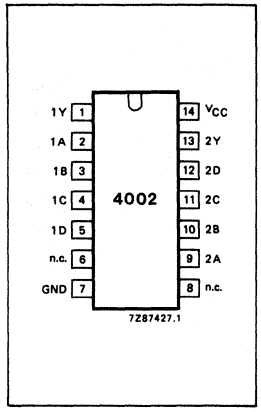

643
1 DIR
2 A0
3 A1
4 A2
5 A3
6 A4
7 A5
8 A6
9 A7
10 GND
20 VCC
19 OE
18 B0
17 B1
16 B2
15 B3
14 B4
13 B5
12 B6
11 B7
7Z90992

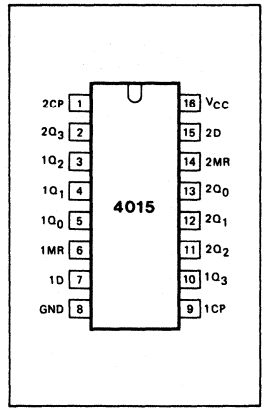

646
1 CPAB
2 SAB
3 DIR
4 A0
5 A1
6 A2
7 A3
8 A4
9 A5
10 A6
11 A7
12 GND
24 VCC
23 CPBA
22 SBA
21 OE
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
7Z93917

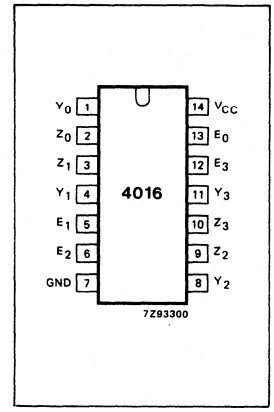

648
1 CPAB
2 SAB
3 DIR
4 A0
5 A1
6 A2
7 A3
8 A4
9 A5
10 A6
11 A7
12 GND
24 VCC
23 CPBA
22 SBA
21 OE
20 B0
19 B1
18 B2
17 B3
16 B4
15 B5
14 B6
13 B7
7Z93927

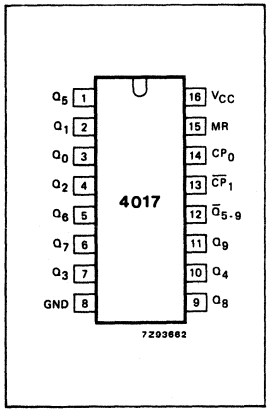

670
1 D1
2 D2
3 D3
4 RB
5 RA
6 Q3
7 Q2
8 GND
16 VCC
15 D0
14 WA
13 WB
12 WE
11 RE
10 Q0
9 Q1
7Z93910

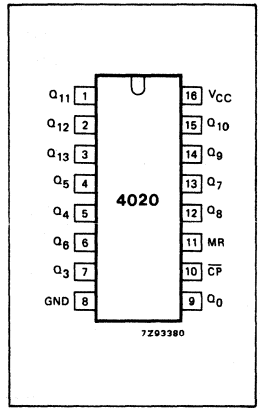

688
$\overline{E}$ 1
P_0 2
Q_0 3
P_1 4
Q_1 5
P_2 6
Q_2 7
P_3 8
Q_3 9
GND 10
20 V_{CC}
19 $\overline{P=Q}$
18 Q_7
17 P_7
16 Q_6
15 P_6
14 Q_5
13 P_5
12 Q_4
11 P_4
7Z87469

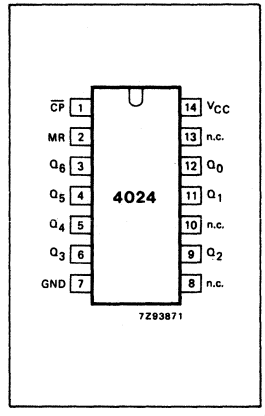

4002
1Y 1
1A 2
1B 3
1C 4
1D 5
n.c. 6
GND 7
14 V_{CC}
13 2Y
12 2D
11 2C
10 2B
9 2A
8 n.c.
7Z87427.1

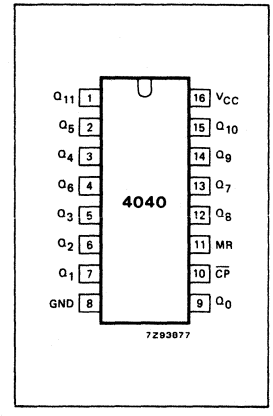

4015
2CP 1
$2Q_3$ 2
$1Q_2$ 3
$1Q_1$ 4
$1Q_0$ 5
1MR 6
1D 7
GND 8
16 V_{CC}
15 2D
14 2MR
13 $2Q_0$
12 $2Q_1$
11 $2Q_2$
10 $1Q_3$
9 1CP

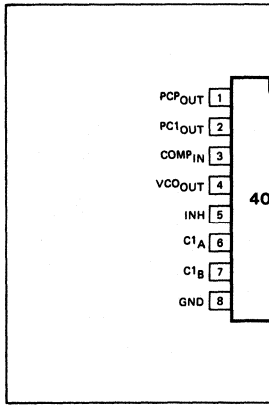

4016
Y_0 1
Z_0 2
Z_1 3
Y_1 4
E_1 5
E_2 6
GND 7
14 V_{CC}
13 E_0
12 E_3
11 Y_3
10 Z_3
9 Z_2
8 Y_2
7Z93300

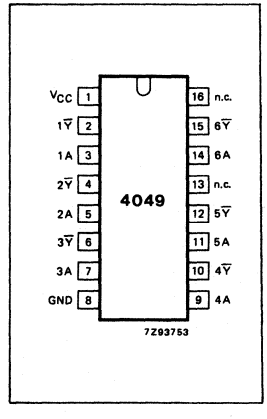

4017
Q_5 1
Q_1 2
Q_0 3
Q_2 4
Q_6 5
Q_7 6
Q_3 7
GND 8
16 V_{CC}
15 MR
14 CP_0
13 $\overline{CP}_1$
12 $\overline{Q}_{5\text{-}9}$
11 Q_9
10 Q_4
9 Q_8
7Z93662

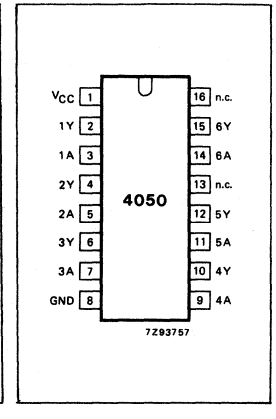

4020
Q_{11} 1
Q_{12} 2
Q_{13} 3
Q_5 4
Q_4 5
Q_6 6
Q_3 7
GND 8
16 V_{CC}
15 Q_{10}
14 Q_9
13 Q_7
12 Q_8
11 MR
10 $\overline{CP}$
9 Q_0
7Z93380

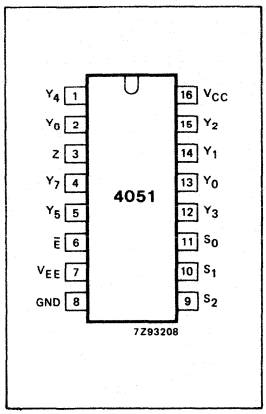

4024
$\overline{CP}$ 1
MR 2
Q_6 3
Q_5 4
Q_4 5
Q_3 6
GND 7
14 V_{CC}
13 n.c.
12 Q_0
11 Q_1
10 n.c.
9 Q_2
8 n.c.
7Z93871

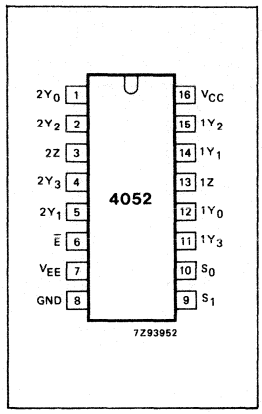

4040
Q_{11} 1
Q_5 2
Q_4 3
Q_6 4
Q_3 5
Q_2 6
Q_1 7
GND 8
16 V_{CC}
15 Q_{10}
14 Q_9
13 Q_7
12 Q_8
11 MR
10 $\overline{CP}$
9 Q_0
7Z93877

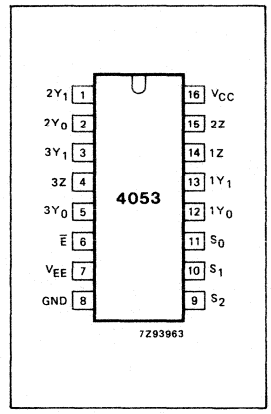

4046A
PCP_{OUT} 1
$PC1_{OUT}$ 2
$COMP_{IN}$ 3
VCO_{OUT} 4
INH 5
$C1_A$ 6
$C1_B$ 7
GND 8
16 V_{CC}
15 $PC3_{OUT}$
14 SIG_{IN}
13 $PC2_{OUT}$
12 R_2
11 R_1
10 DEM_{OUT}
9 VCO_{IN}
7Z96023

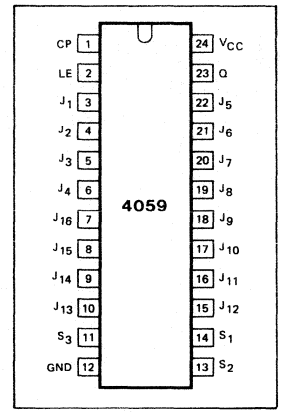

4049
V_{CC} 1
$1\overline{Y}$ 2
1A 3
$2\overline{Y}$ 4
2A 5
$3\overline{Y}$ 6
3A 7
GND 8
16 n.c.
15 $6\overline{Y}$
14 6A
13 n.c.
12 $5\overline{Y}$
11 5A
10 $4\overline{Y}$
9 4A
7Z93753

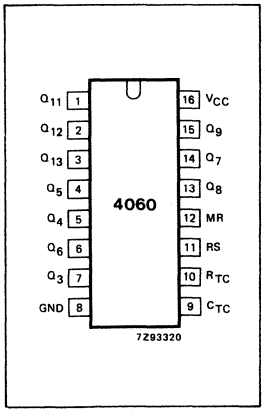

4050
V_{CC} 1
1Y 2
1A 3
2Y 4
2A 5
3Y 6
3A 7
GND 8
16 n.c.
15 6Y
14 6A
13 n.c.
12 5Y
11 5A
10 4Y
9 4A
7Z93757

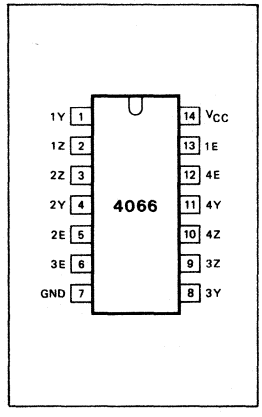

4051
Y4 1
Y0 2
Z 3
Y7 4
Y5 5
E 6
VEE 7
GND 8
16 VCC
15 Y2
14 Y1
13 Y0
12 Y3
11 S0
10 S1
9 S2
7Z93208

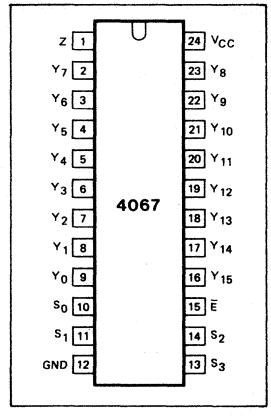

4052
2Y0 1
2Y2 2
2Z 3
2Y3 4
2Y1 5
E 6
VEE 7
GND 8
16 VCC
15 1Y2
14 1Y1
13 1Z
12 1Y0
11 1Y3
10 S0
9 S1
7Z93952


4053
2Y1 1
2Y0 2
3Y1 3
3Z 4
3Y0 5
E 6
VEE 7
GND 8
16 VCC
15 2Z
14 1Z
13 1Y1
12 1Y0
11 S0
10 S1
9 S2
7Z93963


4059
CP 1
LE 2
J1 3
J2 4
J3 5
J4 6
J16 7
J15 8
J14 9
J13 10
S3 11
GND 12
24 VCC
23 Q
22 J5
21 J6
20 J7
19 J8
18 J9
17 J10
16 J11
15 J12
14 S1
13 S2


4060
Q11 1
Q12 2
Q13 3
Q5 4
Q4 5
Q6 6
Q3 7
GND 8
16 VCC
15 Q9
14 Q7
13 Q8
12 MR
11 RS
10 RTC
9 CTC
7Z93320


4066
1Y 1
1Z 2
2Z 3
2Y 4
2E 5
3E 6
GND 7
14 VCC
13 1E
12 4E
11 4Y
10 4Z
9 3Z
8 3Y


4067
Z 1
Y7 2
Y6 3
Y5 4
Y4 5
Y3 6
Y2 7
Y1 8
Y0 9
S0 10
S1 11
GND 12
24 VCC
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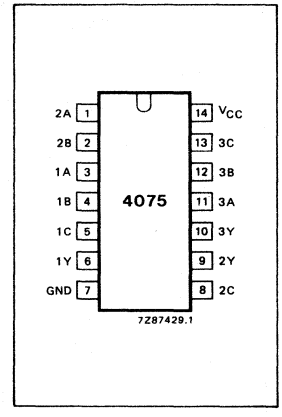
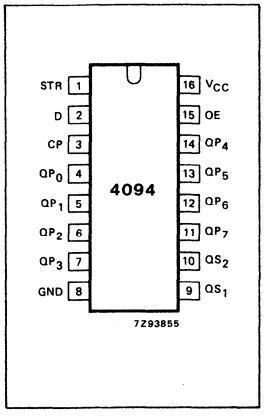
22 Y9
21 Y10
20 Y11
19 Y12
18 Y13
17 Y14
16 Y15
15 E
14 S2
13 S3


4075
2A 1
2B 2
1A 3
1B 4
1C 5
1Y 6
GND 7
14 VCC
13 3C
12 3B
11 3A
10 3Y
9 2Y
8 2C
7Z87429.1


4094
STR 1
D 2
CP 3
QP0 4
QP1 5
QP2 6
QP3 7
GND 8
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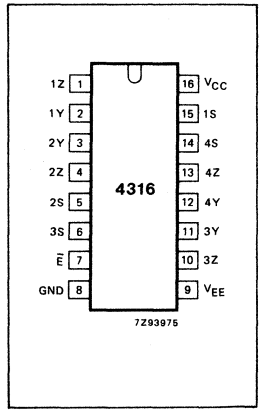
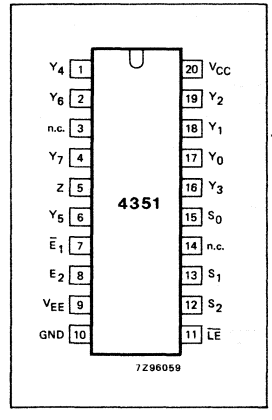
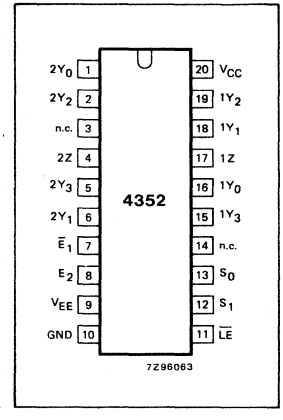
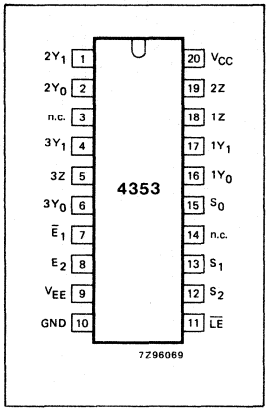
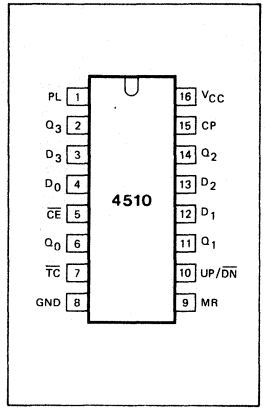
15 OE
14 QP4
13 QP5
12 QP6
11 QP7
10 QS2
9 QS1
7Z93855

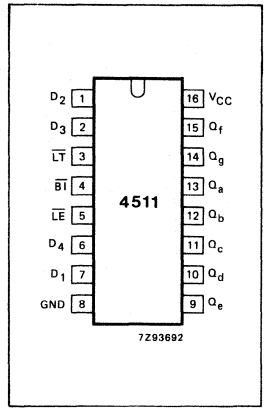

4316
1Z 1
1Y 2
2Y 3
2Z 4
2S 5
3S 6
E 7
GND 8
16 VCC
15 1S
14 4S
13 4Z
12 4Y
11 3Y
10 3Z
9 VEE
7Z93975

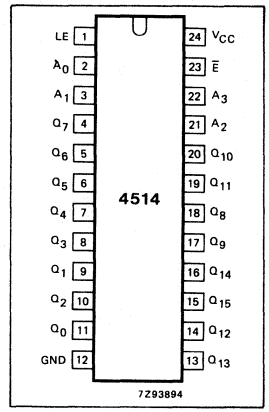

4351
Y4 1
Y6 2
n.c. 3
Y7 4
Z 5
Y5 6
E1 7
E2 8
VEE 9
GND 10
20 VCC
19 Y2
18 Y1
17 Y0
16 Y3
15 S0
14 n.c.
13 S1
12 S2
11 LE
7Z96059

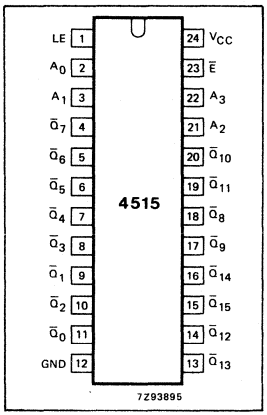

4352
2Y0 1
2Y2 2
n.c. 3
2Z 4
2Y3 5
2Y1 6
E1 7
E2 8
VEE 9
GND 10
20 VCC
19 1Y2
18 1Y1
17 1Z
16 1Y0
15 1Y3
14 n.c.
13 S0
12 S1
11 LE
7Z96063

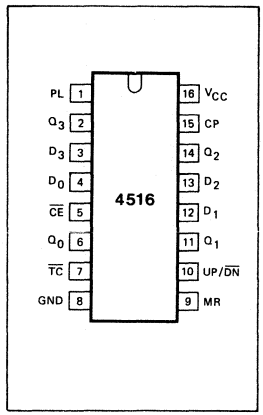


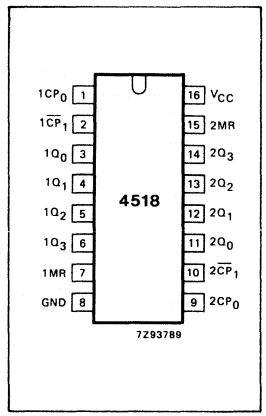


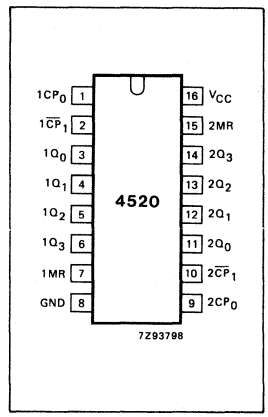


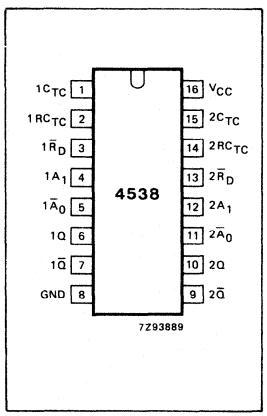


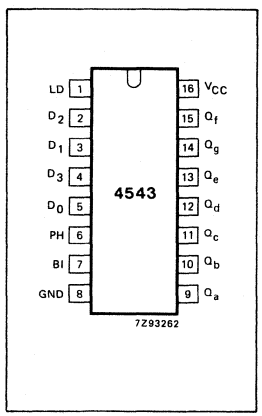






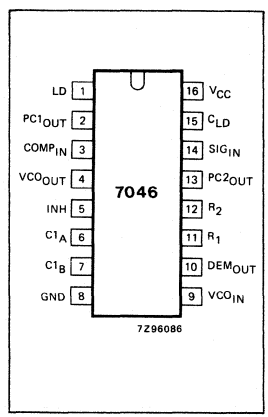


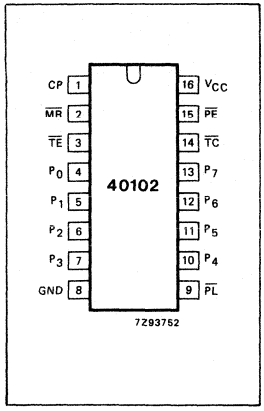


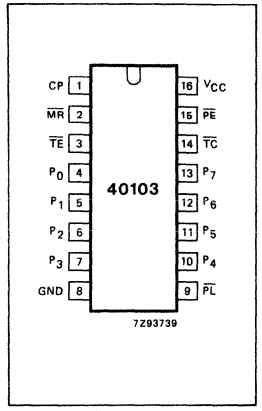


7030

(see next page)




40102
CP 1
MR 2
TE 3
P0 4
P1 5
P2 6
P3 7
GND 8
16 VCC
15 PE
14 TC
13 P7
12 P6
11 P5
10 P4
9 PL
7Z93752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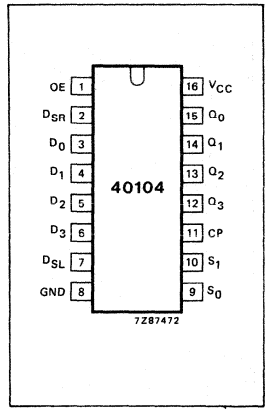
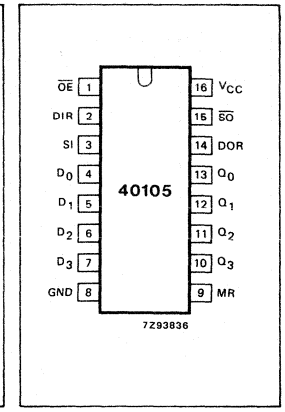
CP 1
MR 2
TE 3
P0 4
P1 5
P2 6
P3 7
GND 8
16 VCC
15 PE
14 TC
13 P7
12 P6
11 P5
10 P4
9 PL
7Z93739


40104
OE 1
DSR 2
D0 3
D1 4
D2 5
D3 6
DSL 7
GND 8
16 VCC
15 Q0
14 Q1
13 Q2
12 Q3
11 CP
10 S1
9 S0
7Z87472


40105
OE 1
DIR 2
SI 3
D0 4
D1 5
D2 6
D3 7
GND 8
16 VCC
15 SO
14 DOR
13 Q0
12 Q1
11 Q2
10 Q3
9 MR
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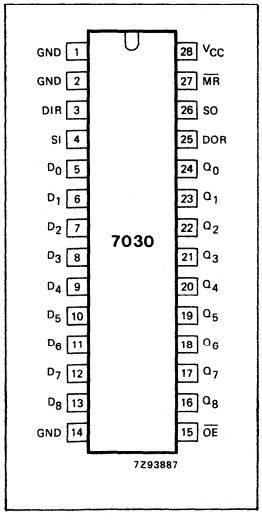

7030
GND 1
GND 2
DIR 3
SI 4
D0 5
D1 6
D2 7
D3 8
D4 9
D5 10
D6 11
D7 12
D8 13
GND 14
28 VCC
27 MR
26 SO
25 DOR
24 Q0
23 Q1
22 Q2
21 Q3
20 Q4
19 Q5
18 Q6
17 Q7
16 Q8
15 OE
7Z93887

NOTES

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current – standard outputs – bus driver outputs		 25 35	 mA mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with: – standard outputs – bus driver outputs		 50 70	 mA mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic DIL		 500	 mW	for temperature range: −40 to +125 °C 74HC/HCT/HCU above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 11 V is specified as the maximum operating voltage.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 6.0$ mA $-I_O = 7.8$ mA
V_{OL}	LOW level output voltage all outputs		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
V_{OL}	LOW level output voltage bus driver outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 6.0$ mA $I_O = 7.8$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
I_{CC}	quiescent supply current **SSI** **flip-flops** **MSI**			 2.0 4.0 8.0		 20.0 40.0 80.0		 40.0 80.0 160.0	 μA μA μA	 6.0 6.0 6.0	 V_{CC} or GND	 $I_O = 0$ $I_O = 0$ $I_O = 0$

FAMILY SPECIFICATIONS

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.
However, to be totally safe, it is desirable to take handling precautions into account (see also chapter "HANDLING PRECAUTIONS").

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 10 V is specified as the maximum operating voltage.

RECOMMENDED OPERATING CONDITIONS FOR 74HCU

SYMBOL	PARAMETER	74HCU			UNIT	CONDITIONS
		min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	V	
V_I	DC input voltage range	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	°C	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current — standard outputs — bus driver outputs		 25 35	 mA mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current for types with: — standard outputs — bus driver outputs		 50 70	 mA mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package plastic DIL		 500	 mW	for temperature range: −40 to +125 °C 74HC/HCT/HCU above +70 °C: derate linearly with 8 mW/K
	plastic mini-pack (SO)		400	mW	above +70 °C: derate linearly with 6 mW/K

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 11 V is specified as the maximum operating voltage.

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage all outputs	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage standard outputs	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 6.0$ mA
V_{OL}	LOW level output voltage all outputs		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage standard outputs		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
V_{OL}	LOW level output voltage bus driver outputs		0.16	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 6.0$ mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$
I_{CC}	quiescent supply current **SSI** **flip-flops** **MSI**			 2.0 4.0 8.0		 20.0 40.0 80.0		 40.0 80.0 160.0	 μA μA μA	 5.5 5.5 5.5	 V_{CC} or GND	 $I_O = 0$ $I_O = 0$ $I_O = 0$
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} −2.1 V	other inputs at V_{CC} or GND; $I_O = 0$

Note

1. The additional quiescent supply current per input is determined by the ΔI_{CC} unit load, which has to be multiplied by the unit load coefficient as given in the individual data sheets. For dual supply systems the theoretical worst-case ($V_I = 2.4$ V; $V_{CC} = 5.5$ V) specification is: $\Delta I_{CC} = 0.65$ mA (typical) and 1.8 mA (maximum) across temperature.

FAMILY SPECIFICATIONS

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the "HC-types", will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.
However, to be totally safe, it is desirable to take handling precautions into account (see also chapter "HANDLING PRECAUTIONS").

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

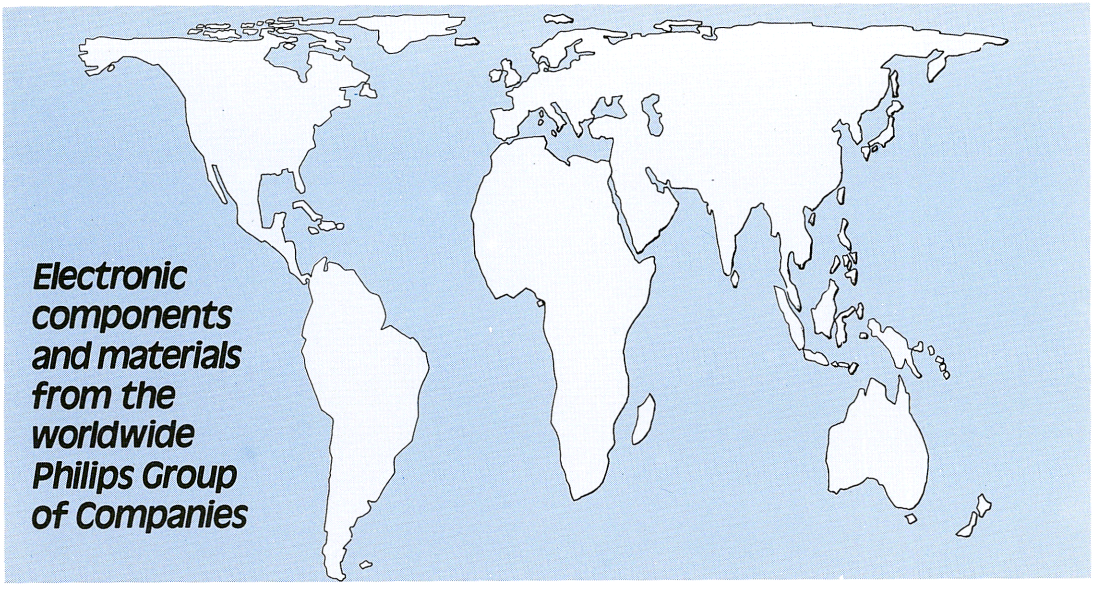
SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

Note

For analog switches, e.g. "4016", "4051 series", "4351 series", "4066" and "4067", 10 V is specified as the maximum operating voltage.

RECOMMENDED OPERATING CONDITIONS FOR 74HCU

SYMBOL	PARAMETER	74HCU			UNIT	CONDITIONS
		min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	V	
V_I	DC input voltage range	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	°C	



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